Educational Administration: Theory and Practice
2024, 30(3), 3657-3664
ISSN: 2148-2403
https://kuey.net/
Research Article

Advanced VLSI Physical Design Optimization: Conceptual Models and Approaches

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Citation: Darshan M. Patel et al (2024). Advanced VLSI Physical Design Optimization: Conceptual Models And Approaches, *Educational Administration: Theory and Practice*, 30(3) 3657-3664
Doi: 10.53555/kuey.v30i3.11338

ARTICLE INFO

ABSTRACT

The rapid scaling of Very Large Scale Integration (VLSI) technology has significantly increased the complexity of physical design, necessitating more advanced and adaptive optimization techniques. Physical design stages such as placement, routing, floor planning, and clock tree synthesis critically influence chip performance, power efficiency, and manufacturability. Traditional heuristic and analytical approaches often face limitations when dealing with mixed-size designs, high congestion, and stringent timing constraints in modern nanoscale technologies. This conceptual paper examines advanced physical design optimization models with a focus on integrated frameworks, machine learning-driven methodologies, and graph-based approaches. It synthesizes existing research to highlight how hybrid optimization strategies combining analytical models with artificial intelligence can address scalability, multi-objective optimization, and design adaptability challenges. The study also identifies key research gaps and outlines future directions for developing unified, intelligent, and scalable physical design frameworks capable of meeting next-generation VLSI design requirements.

Keywords: *VLSI Physical Design, Placement and Routing Optimization, Machine Learning in EDA, Graph-Based Optimization, Integrated Physical Design Frameworks*

1. Introduction

The continuous advancement of Very Large Scale Integration (VLSI) technology has driven the need for highly efficient and optimized physical design methodologies. Physical design optimization, encompassing placement, routing, and floor planning, is a critical step in ensuring high performance, low power consumption, and reduced chip area in modern integrated circuits. As circuit complexity increases, traditional heuristic and analytical methods often struggle to deliver high-quality solutions within reasonable computation time, highlighting the importance of exploring advanced optimization approaches (Patel & Shah, 2024).

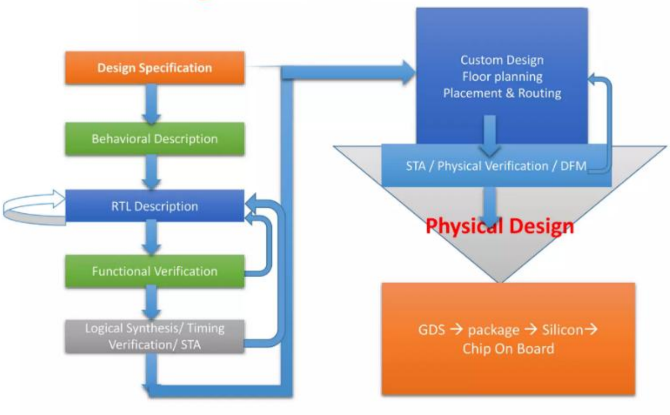

Fig 1: Design flow in VLSI
Source: https://www.slideshare.net/slideshow/physical-design-41787809/41787809#4

Recent research has focused on accelerating placement optimization to enhance VLSI design efficiency. Novel strategies leveraging iterative algorithms, force-directed methods, and timing-driven placement have shown promising results in reducing wire length, improving routability, and minimizing congestion in large-scale circuits (Qiu et al., 2023). Furthermore, the integration of graph-based methodologies has emerged as an effective approach for fast and scalable chip design, allowing placement algorithms to capture complex interconnect dependencies and spatial constraints more accurately (Mirhoseini et al., 2021).
In parallel, machine learning techniques are increasingly being applied to electronic design automation (EDA) to address the limitations of conventional methods. By learning from historical design data, predictive models and reinforcement learning frameworks can guide placement and routing decisions, optimize design parameters, and improve overall solution quality (Huang et al., 2021). These developments collectively suggest a shift towards hybrid approaches that combine conceptual optimization models with intelligent computational techniques, providing a more adaptive and efficient framework for advanced VLSI physical design.
Overall, the evolution of VLSI physical design optimization reflects a trend towards integrating computational intelligence, graph-theoretic models, and algorithmic innovations to meet the challenges posed by complex modern circuits. This emphasizes the need for comprehensive conceptual frameworks capable of guiding both research and practical implementations in next-generation chip design.

1.1 Background of VLSI Physical Design

VLSI physical design is a critical phase in integrated circuit development that translates logical designs into geometrical representations on silicon. This stage encompasses placement, routing, floor planning, and optimization, directly affecting the chip’s performance, power efficiency, and manufacturability. Traditional placement methods, often heuristic or analytical, focus on minimizing wirelength, reducing congestion, and meeting timing constraints. However, the increasing scale and complexity of modern circuits have challenged these conventional approaches, prompting the development of more intelligent and adaptive placement algorithms (Hao, Cai, & Zhou, 2022).

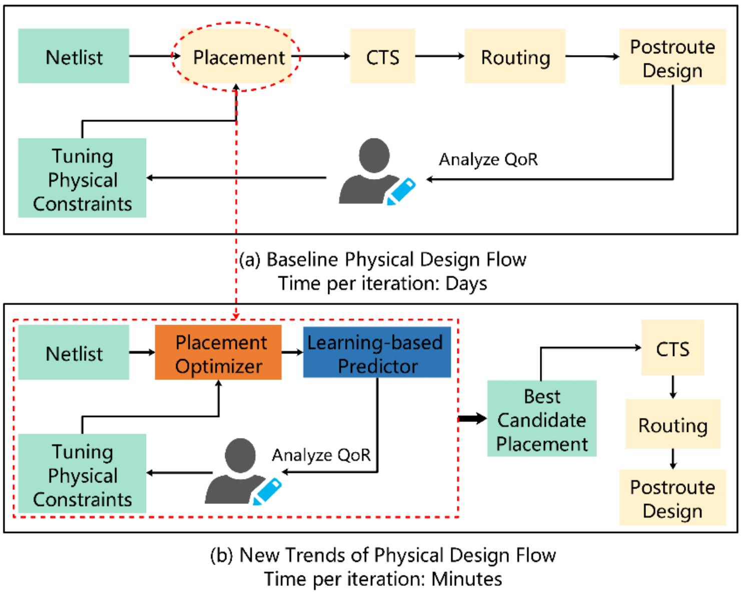

Fig 2: New trends of placement-centric VLSI physical design flow
Source: https://www.mdpi.com/2079-9292/12/2/337

Recent innovations in placement optimization have leveraged advanced computational techniques to improve solution quality and routability. For example, Replace introduced methods to enhance global placement by systematically validating and optimizing routability, demonstrating significant improvements in design efficiency and placement accuracy for mixed-size circuits (Cheng, Kahng, Kang, & Wang, 2019). At the same time, machine learning approaches, particularly deep reinforcement learning, have been applied to placement problems, allowing models to learn optimal strategies from large datasets of prior designs. Such approaches enable more adaptive and scalable solutions that can handle the complexity of modern VLSI circuits while improving wirelength, timing, and congestion simultaneously (Mirhoseini et al., 2020).
These developments highlight a paradigm shift in VLSI physical design, from purely heuristic or rule-based methods to hybrid frameworks that integrate intelligent computational models. By combining traditional optimization principles with learning-based and kernelized techniques, researchers and practitioners are now able to address the growing demands of high-performance, low-power, and densely packed integrated circuits.

1.2 Challenges in Modern Physical Design

Modern VLSI physical design faces numerous challenges due to the increasing complexity of integrated circuits and the demand for higher performance, lower power consumption, and reduced area. One of the primary challenges is handling mixed-size designs, where standard cells, macros, and memory blocks of varying dimensions must be efficiently placed to minimize wirelength and congestion. Dataflow-aware approaches, such as those based on simulated evolution algorithms, have been developed to address placement for mixed-size circuits, yet achieving optimal results while maintaining computational efficiency remains difficult (Lin, Deng, Yang, Chen, & Lu, 2021).

Another significant challenge lies in fixed-outline floor planning, which requires placing all circuit components within a predefined chip area while optimizing for performance metrics. Traditional methods often struggle with the combinatorial complexity of these designs. To overcome this, nature-inspired optimization algorithms, including bio-inspired and particle swarm methods, have been employed to explore large solution spaces efficiently. These techniques improve placement quality and resource utilization but can still face limitations in scalability, convergence speed, and adaptability to new design constraints (Shunmugathammal, Columbus, & Anand, 2020; Ye et al., 2020).

Additionally, modern physical design must contend with timing, thermal, and power constraints simultaneously. Incorporating these multiple objectives into the placement and floor planning process increases computational complexity and demands sophisticated optimization strategies. Despite advances in evolutionary, bio-inspired, and heuristic algorithms, there remains a need for integrated frameworks that can efficiently handle the growing design scale while optimizing across multiple conflicting objectives.

1.3 Scope and Importance of Conceptual Models in Optimization

Conceptual models in VLSI physical design optimization provide a structured framework for understanding, analysing, and improving complex placement and floor planning problems. They allow researchers and designers to abstract intricate circuit interactions and constraints, facilitating systematic exploration of design alternatives while maintaining focus on key performance metrics. Timing-driven placement, for example, benefits from conceptual strategies such as timing-compatibility flip-flop clustering, which organizes circuit elements based on their temporal dependencies, thereby reducing critical path delays and improving overall circuit performance (Mangiras, Stefanidis, Seitanidis, Nicopoulos, & Dimitrakopoulos, 2020).

Robust placement tools like DREAM Place leverage multi-electrostatics-based conceptual frameworks to handle region constraints, mixed-size designs, and congestion-aware optimization. These frameworks provide a foundation for scalable and adaptive algorithms that can efficiently process large industrial designs while balancing competing objectives such as wire length, timing, and routability (Gu, Jiang, Lin, & Pan, 2020; Liao, Liu, Chen, Lv, Lin, & Yu, 2022). Furthermore, integrating deep learning-enabled approaches into global placement highlights the growing relevance of intelligent conceptual models, which enable predictive optimization, adaptive decision-making, and real-time adjustment of placement strategies to meet design specifications (Liu, Sun, Liao, Lin, & Yu, 2021).

Overall, the adoption of conceptual models in VLSI optimization not only enhances solution quality but also accelerates the design cycle by providing a systematic methodology for addressing increasingly complex circuit architectures. These models serve as a critical bridge between theoretical optimization principles and practical implementation in modern electronic design automation workflows.

2. Review of Literature

Author(s)	Year	Aim	Objectives	Scope	Key Findings
Qiu et al.	2023	Analyse placement optimization	Reduce placement runtime, improve quality	Standard VLSI circuits	Progressive methods enhance efficiency and speed
Mirhoseini et al.	2021	Graph-based placement methodology	Improve speed and solution quality	Large-scale chip design	Graph methods reduce runtime and maintain quality
Huang et al.	2021	Survey ML methods in EDA	Review ML for placement, routing, optimization	EDA domain	ML improves efficiency and prediction in VLSI
Hao et al.	2022	Survey intelligent placement methods	Compare heuristic and kernel-based techniques	VLSI placement	Kernelized approaches improve convergence and quality
Cheng et al.	2019	Improve global placement quality	Enhance placement methods	Mixed-size VLSI	Replace improves routability and placement metrics

Mirhoseini et al.	2020	Deep RL for chip placement	Optimize placement using RL	Mixed-size VLSI	RL reduces wirelength and improves performance
Lin et al.	2021	Optimize macro placement	Simulated evolution for macro placement	Mixed-size VLSI	Evolution-based placement improves timing and congestion
Shunmugathammal et al.	2020	Nature-inspired floor planning	Reduce wirelength and area	Fixed-outline VLSI	Nature-inspired algorithms reduce area, improve wirelength
Ye et al.	2020	DPSO for floor planning	Optimize fixed-outline solutions	Fixed-outline VLSI	DPSO improves placement and reduces iterations
Mangiras et al.	2020	Timing-driven placement	Cluster flip-flops for timing	Standard-cell designs	Clustering reduces violations and improves critical path
Gu et al.	2020	Robust placement with electrostatics	Optimize placement with constraints	Mixed-size VLSI	DREAM Place 3.0 improves quality, reduces congestion
Liu et al.	2021	DL-enabled global placement	Optimize routability	Standard-cell VLSI	DL reduces congestion, improves routability
Liao et al.	2022	Timing-driven global placement	Momentum-based net weighting	Standard-cell VLSI	DREAM Place 4.0 improves timing and wirelength
Lin et al.	2021	Remove congestion	Routability-driven global placer	Mixed-size VLSI	Effective congestion removal improves placement
Lu, Pentapati & Lim	2021	Affinity-aware placement	Use GNNs for placement	Mixed-size VLSI	GNNs improve quality, reduce wirelength
Lu & Lim	2020	VLSI placement with GNNs	Apply GNNs to placement	Standard-cell circuits	GNNs outperform classical algorithms
Kirby et al.	2021	RL for placement	Guide global placement	Standard-cell designs	RL reduces wirelength, improves performance
Agnesina et al.	2020	Tool parameter optimization	Deep RL for EDA tools	VLSI flows	Deep RL tunes parameters efficiently
Agnesina, Chang & Lim	2020	Placement parameter optimization	Optimize tool parameters with RL	Standard-cell VLSI	Deep RL improves quality, reduces iterations

2.1 Research Gap

Despite significant advances in VLSI physical design, particularly in placement and floor planning, several research gaps remain. Existing approaches, including heuristic, evolutionary, electrostatics-based, and deep learning methods, have improved placement quality, wire length, and routability, yet they often struggle with scalability and performance in large mixed-size designs. While reinforcement learning and graph neural networks show promise in modelling complex placement dependencies, their practical integration into standard VLSI design flows remains limited. Additionally, timing-driven and congestion-aware optimization techniques are frequently evaluated on benchmark circuits rather than real-world industrial designs, which limits their applicability. Furthermore, most methodologies address specific aspects such as global placement or macro placement independently, without a unified framework that simultaneously considers timing, congestion, and design constraints holistically. This fragmentation indicates a critical need for integrated, scalable, and adaptive optimization frameworks that can generalize across diverse circuit types and technology nodes while leveraging modern computational intelligence techniques.

2.2 Objectives of the Study

1. To examine the evolving challenges associated with modern VLSI physical design optimization.
2. To analyse existing conceptual models and advanced methodologies used in placement, routing, and floor planning.
3. To evaluate the role of integrated optimization frameworks in balancing timing, power, congestion, and routability.
4. To explore the application of machine learning, graph neural networks, and reinforcement learning in physical design automation.
5. To identify research gaps in current VLSI optimization techniques and highlight the need for unified and scalable design frameworks.
6. To propose future research directions for intelligent and adaptive physical design optimization in next-generation VLSI systems.

3. Key Innovations in Physical Design Optimization

The landscape of physical design optimization in VLSI systems has undergone significant transformation in recent years, driven by the increasing complexity of circuits, shrinking technology nodes, and rising performance expectations. Traditional placement and routing methods, while effective for smaller-scale designs, struggle to meet the conflicting objectives of timing, power, routability, and congestion in modern large-scale circuits. Consequently, researchers have developed several innovative approaches that combine analytical modelling, heuristic optimization, and artificial intelligence to enhance design quality and efficiency.

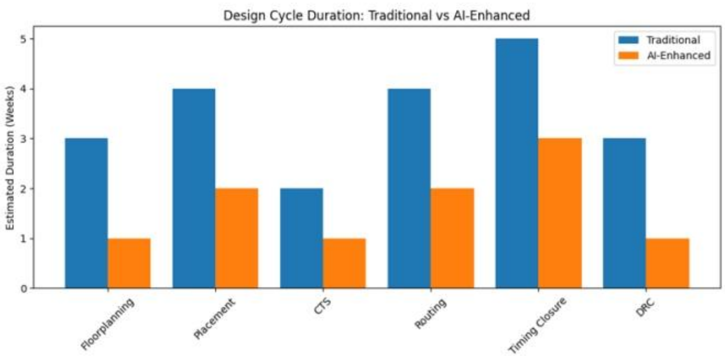

Fig 3: Design cycle duration
Source: https://www.design-reuse.com/article/61623-ai-in-vlsi-physical-design-opportunities-and-challenges/

3.1 Integrated Frameworks for Physical Design Optimization

Integrated frameworks in VLSI physical design aim to unify multiple design objectives such as wirelength minimization, timing closure, congestion management, and routability within a single optimization process. Traditional placement and routing approaches often handle these objectives separately, which can result in suboptimal solutions and require repeated iterations. In contrast, integrated frameworks evaluate multiple metrics simultaneously, enabling designers to achieve a more balanced and robust optimization outcome (Lin et al., 2021).
For example, routability-driven global placement incorporates congestion prediction directly into the placement stage, allowing designers to anticipate routing challenges and reduce the likelihood of timing violations. These frameworks employ iterative algorithms that refine designs progressively, balancing local factors such as cell alignment and proximity with global goals like overall wirelength reduction. By considering interdependent design factors together, integrated approaches improve manufacturability, enhance robustness, and reduce the need for costly post-placement adjustments. Furthermore, their adaptability to various design scales from small standard-cell layouts to large mixed-size chips and across different technology nodes underscores their central role in modern physical design optimization.

3.2 Leveraging Machine Learning for Optimization

Machine learning (ML) has emerged as a transformative tool in physical design, enabling predictive, adaptive, and data-driven optimization. Graph neural networks (GNNs), for instance, model circuits as graphs to capture both spatial layout and connectivity information, allowing the optimizer to understand complex interdependencies among cells. Affinity-aware placement techniques use GNNs to cluster related cells, reducing wirelength and alleviating congestion simultaneously (Lu, Pentapati, & Lim, 2021; Lu & Lim, 2020).
Reinforcement learning (RL) further enhances optimization by learning the impact of placement decisions over successive iterations. An RL agent explores multiple placement options, receives feedback based on key metrics

such as timing and routability, and adjusts strategies to improve overall performance (Kirby et al., 2021; Agnesina, Pentapati, & Lim, 2020). Integrating ML into placement tools provides several benefits: it accelerates optimization, improves robustness across designs and technology nodes, and adapts dynamically to iterative workflow changes. Consequently, ML-based methods are increasingly essential for handling the complexity and scale of modern VLSI circuits, outperforming conventional heuristic-based approaches.

3.3 Advanced Interconnect Design Strategies

Interconnect design has become a critical factor limiting performance in modern VLSI systems, especially as feature sizes shrink and chip densities increase. Advanced interconnect strategies focus on optimizing the distribution and routing of nets to minimize delay, reduce crosstalk, and enhance signal integrity. These strategies often incorporate predictive models that anticipate congestion and signal delays, enabling more efficient routing decisions early in the placement stage (Lin et al., 2021).
Machine learning techniques are also being applied to interconnect optimization, analysing historical placement and routing data to predict congested regions, identify critical nets, and propose placement adjustments that improve performance and manufacturability. Iterative refinement methods further enhance interconnect quality by continuously adjusting placement based on simulated routing outcomes, ensuring high-density regions do not suffer from excessive congestion and timing remains within specifications. By combining predictive modelling, ML-based guidance, and iterative refinement, advanced interconnect strategies play a key role in improving the efficiency, reliability, and performance of modern physical design workflows, particularly for mixed-size and heterogeneous chip architectures.

3.4 Optimization of Clock Tree Networks

Clock tree networks are critical for maintaining synchronized operation across VLSI circuits, and their optimization directly impacts timing, power, and overall performance. Modern clock tree synthesis techniques focus on minimizing skew and delay while balancing load distribution across multiple clock sinks. Traditional methods often optimize clock trees separately from placement, leading to timing discrepancies and higher power consumption. Integrated optimization approaches, however, consider clock tree design alongside placement and routing to achieve more accurate timing closure (Lin et al., 2021).

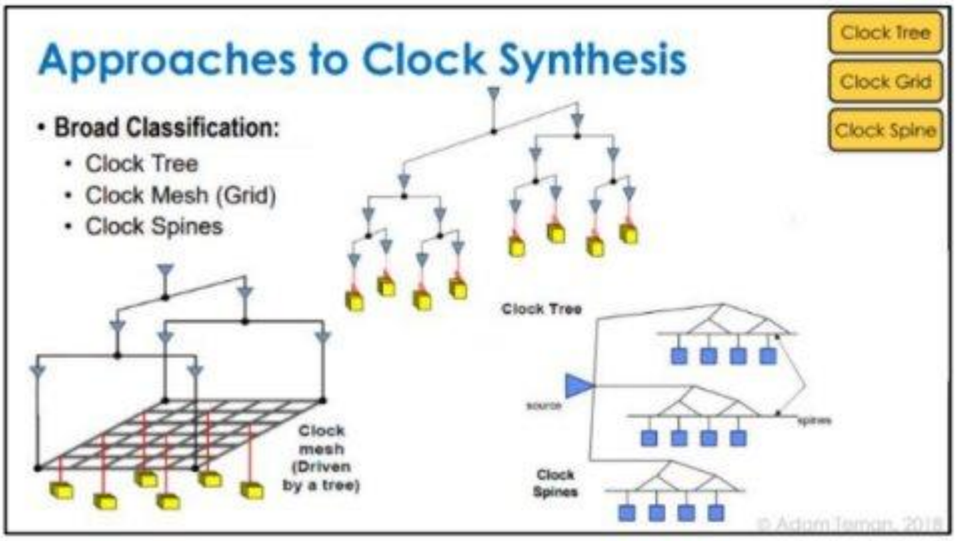

Fig 4: Clock Tree Classification
Source: https://www.design-reuse.com/article/61452-understanding-the-importance-of-prerequisites-in-the-vlsi-physical-design-stage/

Machine learning and analytical models have further improved clock tree optimization. ML models can predict the effects of placement changes on clock skew, enabling designers to adjust cell placement proactively to maintain balanced timing. Reinforcement learning approaches can iteratively refine the clock network, minimizing skew and delay while optimizing power consumption. Such dynamic, data-driven approaches outperform conventional heuristic methods, especially in complex multi-core and high-frequency circuits (Lu, Pentapati, & Lim, 2021).
Finally, clock tree optimization is essential for energy-efficient design. A well-optimized clock network reduces unnecessary toggling and dynamic power consumption, contributing to low-power operation critical for modern portable and high-performance systems. By combining integrated frameworks, ML, and predictive modelling, clock tree optimization ensures reliable timing, energy efficiency, and improved overall performance in contemporary VLSI design.

Future Scope

The future of VLSI physical design optimization is moving toward intelligent, unified, and scalable frameworks that can handle the growing complexity of advanced semiconductor technologies. A key direction is integrating machine learning techniques, such as graph neural networks and reinforcement learning, into traditional EDA flows for predictive and adaptive optimization of placement, routing, and timing (Huang et al., 2021; Lu & Lim, 2020). Another focus is the holistic co-optimization of placement, routing, clock tree synthesis, and power delivery, which can reduce design iterations and improve overall robustness (Lin et al., 2021; Gu et al., 2020). Future work should also emphasize scalability across diverse circuits, technology nodes, and heterogeneous architectures like chiplets and 3D ICs (Mirhoseini et al., 2021; Qiu et al., 2023). Additionally, data-driven parameter tuning and autonomous design-space exploration can minimize manual intervention and enhance efficiency (Agnesina et al., 2020). Progress in VLSI optimization will rely on combining conceptual modelling, computational intelligence, and practical validation.

Conclusion

This study examined advanced approaches to VLSI physical design optimization, highlighting the role of integrated frameworks and intelligent computational models in addressing modern design challenges. As circuits grow in size and complexity, traditional heuristic methods struggle to achieve optimal performance, power efficiency, and routability. Literature shows that hybrid approaches combining analytical optimization with machine learning and graph-based techniques improve placement quality, congestion reduction, and timing closure (Cheng et al., 2019; Hao et al., 2022). Emerging methods such as deep reinforcement learning and graph neural networks enable adaptive, data-driven decision-making, learning complex interdependencies and dynamically adjusting strategies (Mirhoseini et al., 2020; Lu, Pentapati, & Lim, 2021). However, practical integration into industrial flows remains limited, highlighting the need for further research. Overall, the future of VLSI design lies in unified, scalable, and intelligent frameworks that enhance efficiency, reduce development time, and support high-performance next-generation ICs (Patel & Shah, 2024; Qiu et al., 2023).

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