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Design And Validation Of A 32-Bit RISC-V Processor Incorporating Vedic Mathematics

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ARTICLE INFO

ABSTRACT

A Vedic multiplier architecture is employed in constructing a 32-bit RISC-V processor to enhance speed and reduce computational complexity. It's ALU and MAC units, based on Vedic Sutras, are implemented in Verilog HDL and simulated with the Xilinx design suite, achieving lower power consumption and latency compared to traditional designs. The processor includes conventional components like the Control Unit, Register Bank, Program Counter, and Memory. It can execute up to 16 instructions, making it a powerful option for various computing tasks due to its improved speed, reduced power consumption, and minimized area usage.

Keywords: Reduced Instruction Set Computer, RISC V, Von Neumann architecture, Verilog HDL, Vedic Mathematics, Urdhva-Tiryagbhyam Sutra.

INTRODUCTION:

The RISC-V architecture prioritizes simple instruction sets, enhancing efficient decoding and often resulting in better performance than CISC. This approach, combining straightforward instructions with a microprocessor architecture capable of executing instructions within a few cycles, offers fixed instruction sizes, additional registers, and superior clock utilization, albeit with potentially higher memory and code requirements. Performance gains are typically two to four times greater than those of CISC processors. Designing a 32-bit RISC-V processor using Hardware Description Language involves integrating internal components such as registers, ALUs, memory units, and control units, and can be effectively implemented on FPGA.

Vedic mathematics, using techniques known as sutras, provides rapid solutions to mathematical problems, proving effective within mainstream mathematics rather than as a separate discipline. Multipliers, crucial in processors, especially in digital signal processing and communication (e.g., FFT), benefit from Vedic mathematics. Low power consumption is targeted for logarithmic multipliers, addressing drawbacks in common binary multiplication techniques like array and Booth multiplication. Vedic multipliers, based on the Urdhva Triyagbhyam Sutra, offer efficient alternatives, with research demonstrating their superiority in terms of area, power, and delays compared to traditional methods. High-speed Vedic multipliers enhance DSP operations, facilitating quick calculations.

Reversible circuits further reduce power usage compared to combinational logic circuits, and RTL circuit verification is conducted using property-driven verification. In DSP applications, where multiplication often involves repetitive addition, the Ekadhikena Purvena Sutra simplifies the squaring task. Multipliers generally follow a three-step process: partial product generation (PPG), partial product reduction (PPR), and final addition, with AND gates generating a partial product matrix (PPM) during the PPG stage for unsigned multiplication.

LITERATURE REVIEW:

In "Design and Comparison of Multiplier using Vedic Sutras" by S. Lad and V. S. Bendre, presented at the 2019 5th International Conference On Computing, Communication, Control And Automation (ICCUBEA), the authors highlight the crucial role of rapid processing units in contemporary computational tasks, particularly for real-time applications. These units, featuring Arithmetic Logic Units (ALUs) and Multiply-Accumulate (MAC) units, depend heavily on efficient multipliers to enhance execution speed and accuracy in digital signal processors. Optimization of these components—multipliers, adders, and registers—is essential for performance improvement.

The design and verification of a 16-bit RISC processor by Seung Pyo Jung et al., detailed at the 2008 International SoC Design Conference in Busan, introduces a processor with Harvard architecture, a 24-bit address, and a 5-stage pipeline. This processor, implemented on FPGA, successfully runs the ADPCM vocoder and SOLA algorithm. The need for compact, low-power processors in portable multimedia players (PMPs) and personal digital assistants (PDAs) is addressed by this design, which aims for SOC-level ASIC integration. Despite the widespread use of 8051 and ARM 7 processors, they present limitations in size and calculation time, prompting the development of this new 16-bit RISC processor.

In "Design and Implementation of 16 Bit Processor on FPGA," Balpande Vishwas V et al. describe the creation of a 16-bit RISC processor using Verilog HDL and Harvard architecture. The project ensures a simple instruction set for seamless hardware execution, modeling complex components like the ALU and memory behaviorally, while simpler components like adders are approached structurally. The processor's functionality is verified through simulation, allowing for future expansion to 32 or 64-bit processors with minor code modifications.

F. Adamec and T. Fryza's "Design — Time configurable processor basic structure," presented at the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, introduces a time-configurable processor core, emphasizing its minimal integer core configuration. The project compares this design with similar solutions, such as the Xtensa processor from Tensilica, which offers extendable instruction sets and advanced features like FPU, DSP engines, and multimedia codec acceleration. The Xtensa architecture follows a RISC LOAD/STORE approach and supports VLIW execution, demonstrating flexibility for various computational demands.

METHODOLOGY:

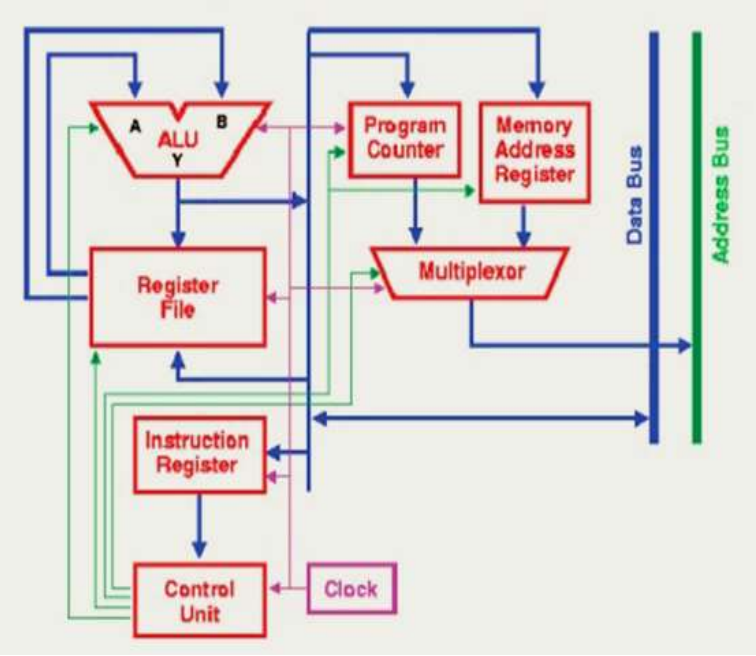

Fig 1: Block diagram of processor

The multiplier unit is an essential component in any processor, forming the foundation for high-speed design techniques as detailed in [13][14]. The Urdhva Tiryagbhyam method was developed for efficient mental calculations by multiplying each row, introducing vertical and crosswise addition and multiplication, and using a straightforward digit from each unit for easy recall.

The Arithmetic Logic Unit (ALU) in a combinational circuit performs various bitwise and arithmetic operations using a set of instructions. In a CPU, the ALU receives an instruction and operands, with the opcode determining the operation to be performed on the operands.

The Control Unit generates control signals to manage resources such as registers and external memory, and to dictate the tasks they perform. In our system, the Control Unit sends control signals to the memory and register blocks for reading or writing data and manages the branching signals based on instruction execution.

The register block contains 32 registers that can store and write 32-bit values from the memory block or ALU in response to control signals. Each register is accessible via a unique address within the memory block.

The memory block serves as external memory, storing 32-bit addressable words. The ALU can read from and write to this block in response to control signals.

The instruction block stores the set of instructions to be executed, while the program counter holds the address of the current instruction. The program counter increments with each clock cycle, pointing to the next instruction's address.

The instruction decoder identifies the type of instruction from the processor's instruction library and assigns the appropriate registers to each part of the instruction. Based on the opcode, it decodes the instruction into various locations and function values.

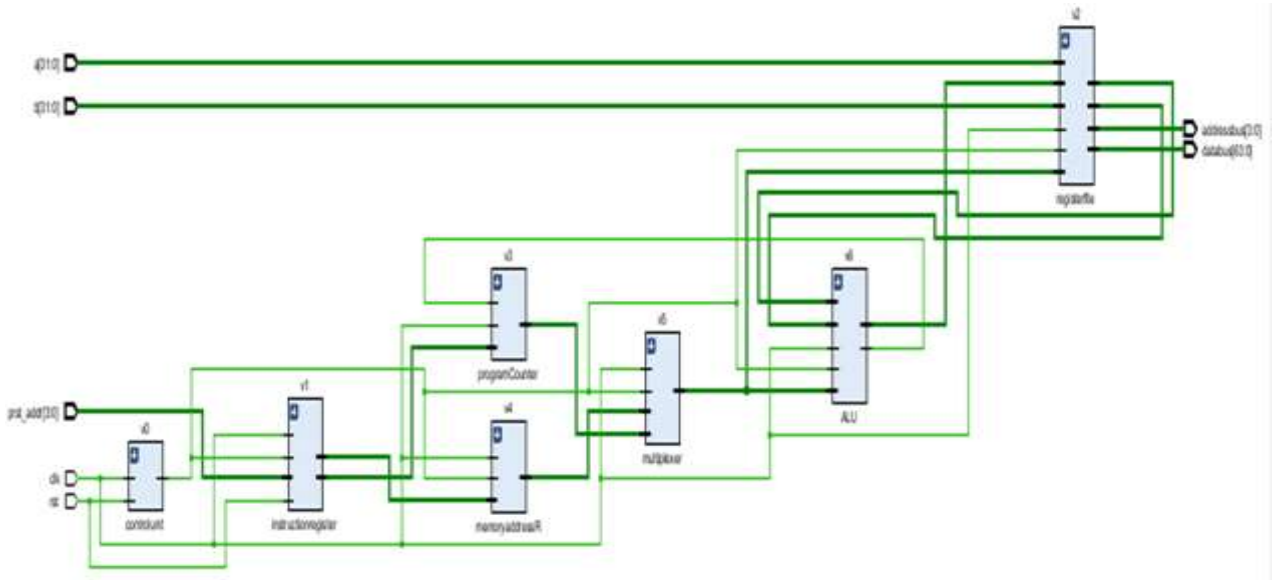

Fig 2: Gate level Netlist

RISC-V Processor Core: Begin by establishing the essential components of a RISC-V processor core, which include the instruction fetch, decode, execute, memory access, and write-back stages. Vedic Multiplier Integration: Integrate the Vedic multiplier into the execution stage of the processor pipeline, adding components that efficiently multiply two operands using Vedic multiplication techniques. Incorporate pipeline registers between stages to ensure the seamless flow of instructions and data throughout the processor pipeline. Design control logic to manage the flow of instructions and data, addressing hazards, stall conditions, and branching effectively. Develop interfaces for accessing instruction and data memory, encompassing the instruction cache, data cache, and main memory.

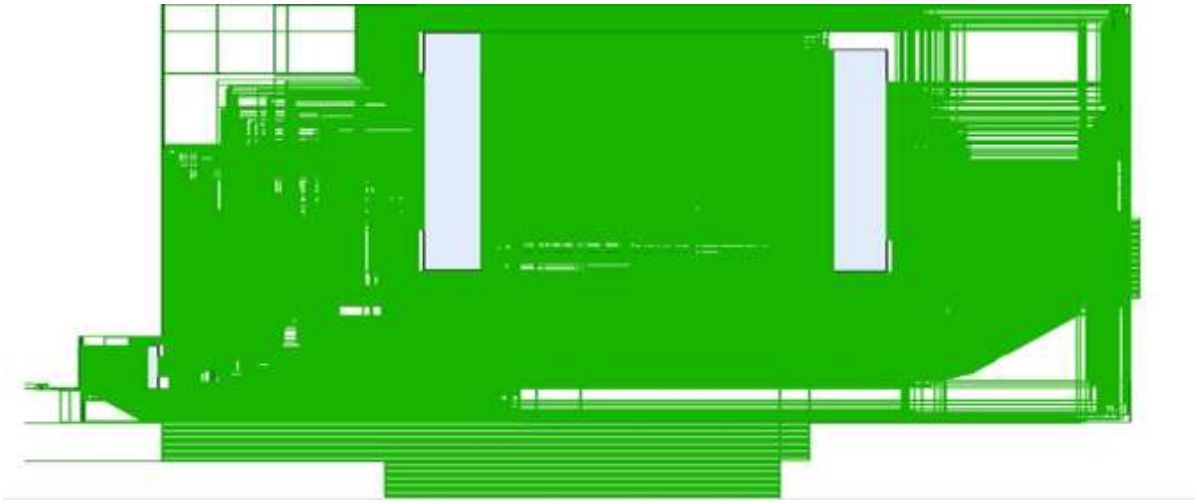

Fig 3: RTL Schematic

This schematic integrates the RISC-V processor's core components with the Vedic multi plier allowing for faster and more precise arithmetic calculations. The 32-bit RISC-V processor featuring a Vedic multiplier utilizes a simplified instruction set architecture (RISC) to perform computations efficiently. The Vedic multiplier, based on ancient Indian mathematics, enhances multiplication operations by breaking them down into smaller, more manageable steps. This schematic integrates the RISC-V processor's core components with the Vedic multiplier.

RESULT:

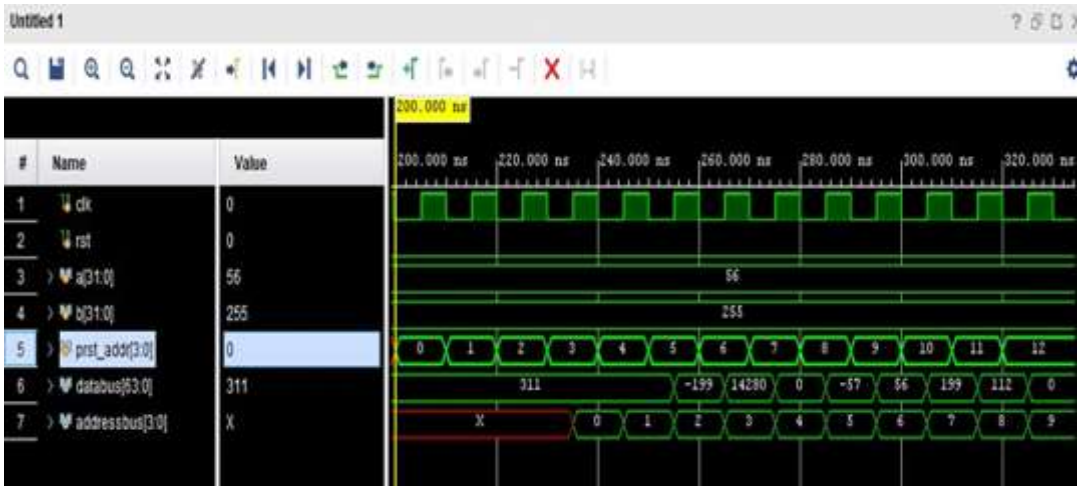

Fig 4: Simulation Results

The waveform output for a 32-bit RISC-V processor utilizing the Vedic multiplier would depict various stages of the processor's operation over time. This includes signals representing instruction fetch, decode, execution, memory access, and write-back stages. Additionally, specific signals related to the Vedic multiplier, such as partial products generation, addition, and accumulation, would be visible. The waveform would showcase the efficient parallel processing capabilities of the Vedic multiplier, resulting in faster multiplication operations compared to traditional methods.

	Area (LUT's)	Delay (ns)
processor	3795	64.549

Fig 5: Evaluation of Area and delay report

CONCLUSION:

This paper details the implementation of a RISC-V processor with an ALU based on Vedic sutras. By using Vedic multipliers, the design enhances multiplication speed while reducing the size and power requirements

of the multipliers. The Vedic processor incorporates standard processor blocks along with Vedic MAC and Vedic ALU units. The architecture supports a 14-instruction set. The performance of the Vedic ALU and MAC is compared with current ALU and MAC results, demonstrating that the 32-bit Vedic processor significantly reduces latency and conserves energy compared to traditional processors. Key features of the RISC-V CPU design include higher operating speed, lower power consumption, and decreased area usage.

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