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**Research Article**

# Analysis Of 8-Bit Counter Using Gdi With Clock Gating For Signal Processing Applications

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**ARTICLE INFO**

**ABSTRACT**

This paper presents the simulation of a 8-Bit Counter using GDI technique and GDI with CLOCKGATING technique .GDI (Gate Diffusion Input) is a new technique of low power digital circuit design and this technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. Clock gating is a popular technique used in many digital circuits for reducing dynamic power dissipation, by removing the clock signal when the circuit is not in use. The 8-bit counter is designed by using T-flip flop based on GDI technique. In this approach conventional GDI counter and GDI with CLOCKGATING based counter has been analyzed in terms of delay, power consumption and power delay product. All these parametric analysis had been carried out using Tanner EDA tool(16.01v). This is better technique when compared to CMOS and GDI existing techniques in terms of Power, Delay and Power delay product.

**Keywords –** T Flip-flop, GDI Technique

## 1.INTRODUCTION

In VLSI technology, it is possible to implement, verify and test the complex, single chip electronic systems, that are the foundation of the day information technology revolution[1].
A digital counter is a machine that produces binary digits in a predetermined count pattern. The counter moves from one number to the next only on a clock pulse, and it progresses through the defined sequence of numbers when activated by an incoming clock waveform. They can count a specific event that occurs in the circuit. Flip-flop circuits are utilized in the design of the counter.

In this, the design of low power counter using GDI with clock gating is focused [2]. The power consumption of counter is improved by using GDI with clock gating technique. The GDI method is based on the utilization of a straightforward cell, as seen in figure 1. The GDI cell has three inputs: P (input to the source/drain of PMOS), G (gate input, common to both PMOS and NMOS), and N (input to the source/drain of NMOS). In contrast to CMOS inverter, the bulk of both NMOS and PMOS are connected to N or P, allowing it to be flexibly biased. Fig.1 shows the basic structure of gate diffusion input cell. With regard to various combinations of the inputs G, P, and N, the GDI cell can produce various Boolean expressions [3].The majority of fundamental logic operations that the GDI approach can realize use fewer transistors.

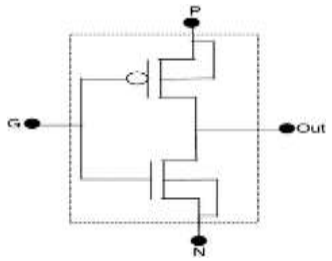


**Fig:1 Basic Gate Diffusion GDI cell.**

Table 1 demonstrates how altering the arrangement of the basic logic cell's G, P, and N inputs can result in drastically diverse Boolean expressions at the output node [4]. Several GDI cells can be combined to create numerous input gates, which can then be used in sequential and combinational circuits for low power signal processing applications.

**Table 1 lists the primary GDI Cell's functions.**

| GDI INPUTS | | | Output of GDI logic | Logic Functionality |
|---|---|---|---|---|
| G | N | P | | |
| A | 0 | B | $A^1B$ | F1 |
| A | B | 1 | $A^1 + B$ | F2 |
| A | B | 0 | AB | AND |
| A | 1 | B | A+B | OR |
| A | 0 | 1 | $A^1$ | NOT |
| A | C | B | $A^1B + AC$ | MUX |

Clock gating is one of the method is shown in fig.2 for conserving the dynamic power of clock components and it works on the premise of stopping the clock of sequential elements whose data is not toggling[5].

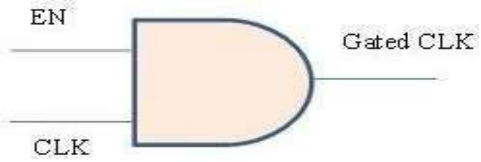


**Fig2: Clock gated circuit.**

This clock gating technique can be used in different sequential circuits means wherever the clock want to disable. The counter can be designed using clock gating technique is shown in fig.3.

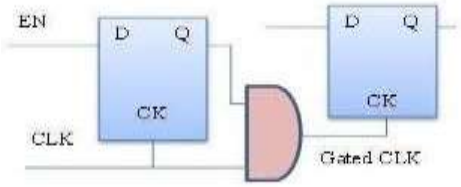


**Fig3: Counter implementation with gate based technology.**

## 2. LITERATURE SURVEY

Dr.K.Nehru and Dr.A.Shanmugam have used Gate diffusion input technique to design low power digital circuits that is used to reduce transistor count and power delay product of the digital circuits. The 16-bit counter is designed by using master-slave flip-flop based on GDI technique.The latency, power consumption, and power delay product of a traditional CMOS counter and a GDI-based counter have been examined in this way. Tanner CAD tool was used to do all of these parametric analyses, with supply voltages ranging from 0.8V to 1.8V. The analysis showed that GDI-based counters are more suited for use as counters in low power applications. -2015

G. Naveen Balaji, R. Prabha, E. Shanthini, J. Jayageetha and MohandLagha have designed flipflops and counters using transmission gate.Sequential circuits like counters play a crucial role in digital systems. Power consumption reduction for these circuits is a top priority. By using transmission gates while designing circuits, power loss, propagation latency, digital circuit area, and design complexity are all decreased. Tanner software is used during the entire design process for sequential circuits and simulations.-2016

U. Kaur and R. Mehragated have minimised the switching power of the signal via a new clock gating flip flop method. It has reduced the number of transistors. The proposed flip-flop is utilised to create a binary counter with 10 bits. This counter has been created up to the layout level utilising 90nm CMOS technology, a 1V power supply, and Microwind simulations. The effectiveness of the new strategy in terms of power usage and transistor count has been demonstrated through simulations. – 2017

Tak-Kei Lam, Xiaoqing Yang, Wai-Chung Tang and Yu-Liang Wu have employed a method called clock gating, which enables shutting down specific clocks during invalid cycles, to further reduce power. Experimental results show that by using the error cancellation technique, a total power (including dynamic and leakage power) cut of up to 23% and in average of around 6% could be stably achieved. These new multi-stage logic error cancellation operations may also be used to solve other sequential logic synthesis issues. The experimental results have showed that applying the Error cancellation technique alone could bring an

average total power cut of about 6% regardless of applying Power Compiler's optimization together or not .- 2018
V. Rajmohan and V. Ranganathan are utilized with reversible logic design, which is more popular due to its low power usage. Reversible circuit design has been extensively studied both sequentially and in combination. They have proposed a reversible T-Flip-flop which is better than the existing designs in the literature. A novel design of reversible asynchronous and synchronous counters are also proposed . As far as is known, this is the first attempt to incorporate reversible logic into the counter architecture. They have also proposed a new reversible gate which can be used as copying gate. – 2018
Biswarup Mukherjee and Aniruddha Ghosal have used a new design of a low power, low latency Wallace tree multiplier. Modern DSP applications frequently use the Wallace Tree algorithm because it can offer a quick and space-efficient method for higher operand multiplication. The addition process of partial products has a longer latency and is more complicated for larger bits of multiplication. In this communication, a variety of strategies are used in the partial products addition circuits to enhance the Wallace multiplier's speed and area delay. Using a 250nm process technology standard CAD tool design compiler, the proposed design is synthesised for 4x4 bit multiplication. According to the findings of the simulation, the proposed multiplier design offers the best power and delay outcomes when compared to other multipliers that are currently in use. – 2019
Priyanka Singh Rana has used a low power design of Johnson counter which provides huge depreciation in the power dissipation. The undesired switching of the clock pulses is suppressed using the clock gating approach. Low power logic gates are used here by utilizing GDI technique. A new design of low power flip-flop is proposed which further accounts for power reduction. Tanner EDA 14.1 is used for simulations using 90nm technology. When compared to the Johnson counter employing clock gating, the proposed solution exhibits a 44% power reduction. – 2020
Chauhan, Jitesh Singh, Chauhan and Ram Chandra Singh have used gate diffusion input (GDI) cell to design an UP-DOWN counter, its performance is evaluated and compared with conventional method-based counters. In the Cadence Virtuoso EDA tool, the circuits are simulated using the industry-standard 90 nm CMOS manufacturing technology. The proposed flip-performance flop's analysis at a 400 MHz clock frequency reveals that its area need is 81.8 m2, its power dissipation is 187.1 nW, and its signal propagation latency is 127.15 ps. Also, the suggested counter consumes 388.2 m2 of IC chip space and dissipates 1040.55 nW of power at 1 GHz clock frequency. – 2021

## 3. DESIGN OF D-FLIPFLOP USING GDI TECHNIQUE

The fig.4 displays the schematic for a D flip-flop made with GDI method. The master and slave latches make up the static D flip-flop. Internal signals are transferred to the outputs when the CLK signal is low [6]. Hold phase is when the CLK signal is high.

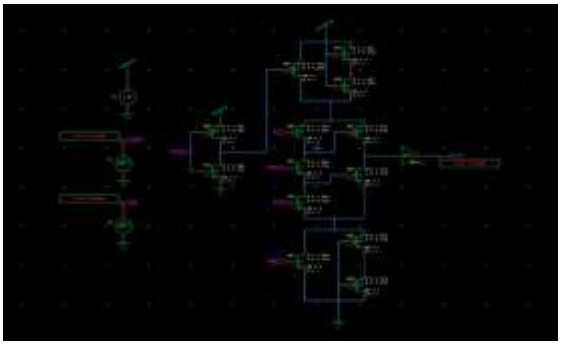

**Fig 4: Schematic for a D flip-flop**

The fig.5 displays the schematic for a XOR gate made with GDI method[7].

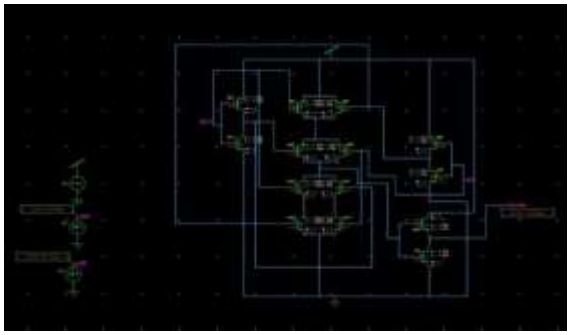

**Fig5: Schematic for a XOR gate**

### A. DESIGN OF T-FLIPFLOP USING GDI TECHNIQUE:

By combining of D-flip-flop and XOR gate will get T-flipflop and it is also called Toggle flip-flop [7]. The schematic diagram for T-flipflop is shown below fig 6. Using this T flip-flop, sequential circuits can be designed. The fig.7 shows the schematic for a 8-bit asynchronous up counter using GDI technique.

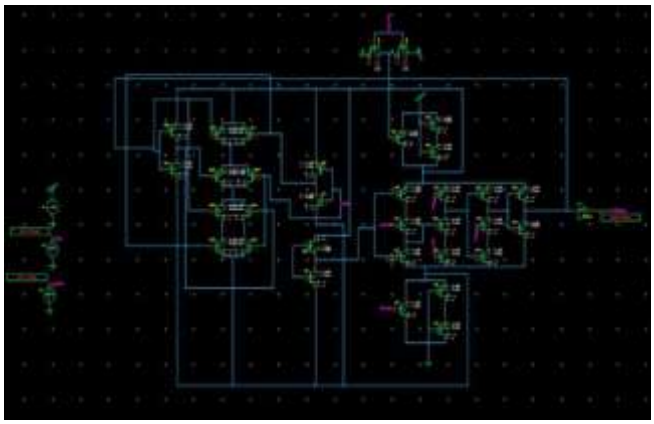

**Fig 6: Schematic for a T flip-flop**

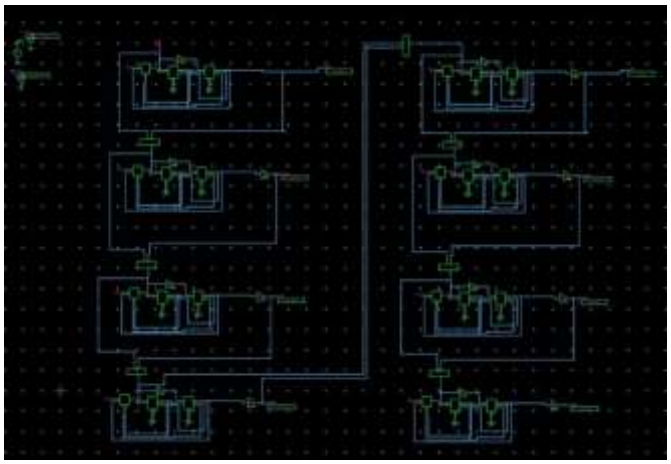

**Fig 7: 8-bit up counter using GDI technique**

### B. Design of 8-bit counter using GDI with CLOCK GATING technique

The term "asynchronous counter" refers to a counter whose flip-flops do not receive the same clock signal [8]. Only the first flip-flop receives the system clock's output as a clock signal. The clock signal is fed to the remaining flip-flops from the output of the flip-flop in the previous stage [9]. Means the clock for the present flip-flop is the output of the previous stage.

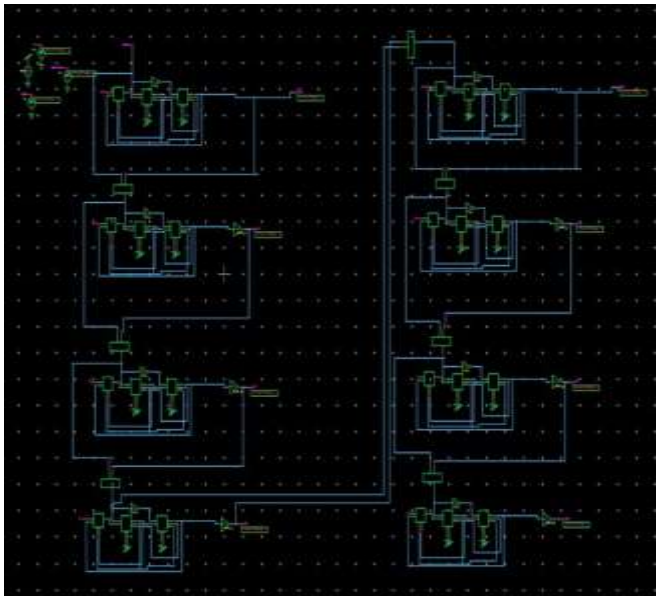

**Fig 8: proposed 8-bit counter using GDI with clock gating.**

## 4. SIMULATION RESULTS AND COMPARISION:

Using Tanner tool, design the asynchronous counter and simulated the same using W-editor. The waveforms are shown in fig 9.

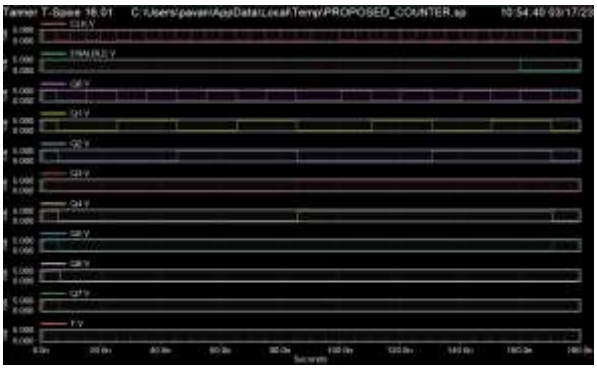

**Fig 9:Waveforms for proposed 8-bit counter using GDI with clock gating.**

After simulation, the different parameters as power and delay for this proposed design were observed and compared these values with existing technology. The comparing values are shown in table 2.

**Table:2 Analysis of power, delay comparing with different techniques.**

| Parameter | Power(mW) | Delay(ns) |
|---|---|---|
| 8-bit normal counter [11] | 14 | 6.033 |
| Exsisting 8-bit counter [11] | 12 | 4.952 |
| Proposed 8-bit counter using gdi technique | 8.6 | 0.523 |
| Proposed 8-bit counter using gdi with clock gating technique | 8.3 | 0.498 |

The comparison results between proposed and existing method is show in fig.10. These results can be showed using bar chart.

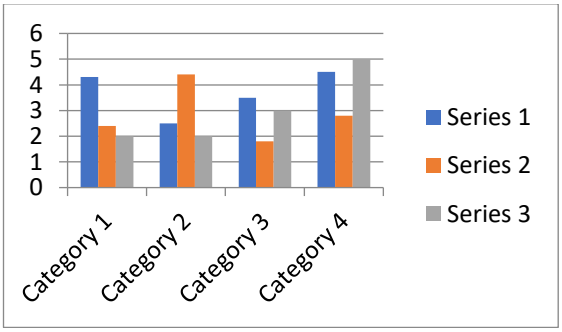


**Fig10. Performance between existing and proposed method.**

## CONCLUSION

This paper proposes the gate diffusion input with clock gating technique to design the counter for achieving power and delay .This is better technique when compared to GDI existing technique in terms of Power and Delay . The power is reduced to 30.8%.Thus this logic style is better platform for designing of sequential circuits.

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