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Research Article

Performance Comparison of 5 and 7 Level Current Fed Inverter for Grid Integrated Solar Plant

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ABSTRACT

Power electronic converters were developed to integrate photovoltaic (PV) arrays with the utility grid. Inverters are essential for converting the direct current produced by PV arrays into alternating currents. Multilevel inverters have significant popularity in PV systems due to their numerous advantages over conventional inverters, particularly in high-power applications. One major benefit is the improvement in output waveforms, as multilevel inverters generate nearly sinusoidal voltage waveforms, resulting in lower total harmonic distortion. Additionally, these inverters experience reduced switching losses, and required the smaller LC filters. In this paper such as current-fed 5-level and 7-level inverters are realized by using Space vector pulse width modulation technique and compare the THD.

Key Words: 5-level, 7-Level Inverter, SVPWM, THD, PV Plant

1.Introduction

Multilevel Current-Fed Inverters (CFIs) [1-5] are becoming popular in power electronics because they produce high-quality outputs, improve efficiency, and reduce harmonic distortion. These advantages make them ideal for applications like solar PV system [6] This paper explores the comparative benefits of the seven-level current-fed converter over the five-level converter, with a particular focus on waveform quality and harmonic distortion. The seven-level converter is designed to generate an output waveform with seven discrete current levels, which allows for a finer approximation of the desired sinusoidal waveform. This increased number of levels contributes to a reduction in the harmonic content present in the output voltage and current.

2. Literature

M. P. Aguirre, L. Calvino, and M. I. Valla (2013) [1] present a multilevel current-source inverter (CSI) controlled by a Field-Programmable Gate Array (FPGA). Their research demonstrates how FPGA control can enhance the performance of multilevel CSIs by providing precise and flexible modulation strategies. The study highlights improvements in output waveform quality, reduced harmonic distortion, and increased system efficiency. This work contributes to the advancement of multilevel inverter technology, showcasing the potential of FPGA-based control in industrial applications requiring high reliability.

N. Binesh and B. Wu (2011) [2] introduce a 5-level parallel current source inverter (CSI) designed for high-power applications with DC current balance control. Their research addresses the challenges of maintaining DC current balance in parallel inverter configurations, ensuring stable and efficient operation. The proposed inverter topology enhances power handling capabilities and reduces harmonic distortion, making it suitable for demanding industrial applications. This work provides significant insights into the development of advanced high-power inverter systems, emphasizing improved performance and reliability through effective current balancing techniques

M. Brenna, R. Faranda and S. Leva, (2010) [3] analyze a novel network topology for high-power grid-connected photovoltaic (PV) systems. Their study focuses on the dynamic performance and stability of the new network design, emphasizing its ability to handle high power levels efficiently. The proposed topology addresses key challenges in integrating large-scale PV systems with the grid, such as power quality and reliability. Their

findings contribute to advancing PV system design by offering solutions that enhance overall system performance and grid compatibility.

Bruno Scortegagna, Dupczak, Arnaldo José Perin, and Marcelo Lobo Heldwein (2012) [4] present a space vector modulation (SVM) strategy applied to interphase transformers-based five-level current source inverters (CSIs). Their research introduces an advanced SVM approach to optimize the performance of these multilevel inverters, improving voltage quality and reducing harmonic distortion. The proposed strategy enhances the operational efficiency and control of the inverter system, making it particularly effective for high-power applications. This work contributes significantly to the field by providing a robust solution for managing complex inverter configurations.

P. P. Dash and M. Kazerani (2012) [5] explore harmonic elimination in a multilevel current-source inverter (CSI)-based grid-connected photovoltaic system. Their study focuses on techniques to reduce harmonic distortion in the output of the inverter, improving the quality of power fed into the grid. By employing advanced harmonic elimination strategies, the authors enhance the efficiency and reliability of photovoltaic systems, making them more compatible with grid requirements. Their work contributes to the development of high-performance renewable energy systems.

3. SVPWM technique for Multilevel Current Fed Inverter

Space Vector Pulse Width Modulation (SVPWM) technology is an advanced method [8-11] used in the control of AC motors and inverters. It generates the required output voltage by converting the desired reference voltage vector into a combination of the nearest three vectors in the inverter's space vector diagram. This technique optimizes the use of the DC bus voltage, reduces harmonic distortion, and improves the overall efficiency of the motor drive. SVPWM is widely used in industrial applications for its superior performance in managing motor speed and torque with high precision and minimal losses
Space Vector Pulse Width Modulation (SVPWM) technology for current-fed inverters is an advanced control method that optimizes the switching sequences of the inverter to achieve efficient power conversion. In current-fed inverters, which maintain a constant current input, SVPWM is used to produce precise output waveforms by determining the optimal combination of space vectors. This results in lower harmonic distortion, improved voltage control, and better utilization of the DC input current. By enhancing the performance and efficiency of current-fed inverters, SVPWM technology is particularly beneficial in applications requiring high power quality and reliable motor control

4. 5-Level Current Fed Inverter

To prevent the presence of low-frequency components in the output current of a multilevel current-fed inverter (CFI), it's essential to select appropriate switching state vectors and ensure effective time sharing among these vectors when employing space vector modulation (SVM) techniques. Additionally, when using the nearest switching method, the switching state vectors are carefully chosen to eliminate low-frequency pulsations in the inverter DC-link voltages. Furthermore, for photovoltaic (PV) or fuel-cell sources, the associated DC-DC converters should be designed to accommodate the wide variation in output voltage.

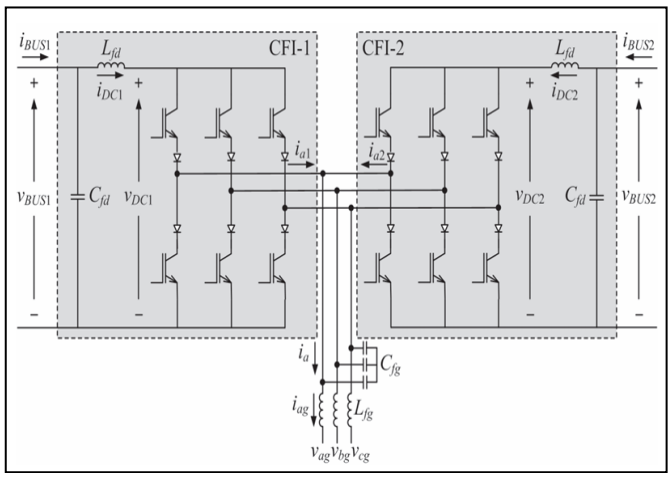


Figure1: 5-Level Current Fed Inverter

The a five-level current-fed inverter. It consists of two three-phase, three-level CFI units as shown in Fig. 1. These CFIs are connected in parallel and share a common Lfg-Cfg filter on the AC-side. Each three-level CFI

unit comprises of six unidirectional switches and a Lfd-Cfd filter on the DC-side. Each module-integrated DC-DC converter produces a continuous current at its output, based on the available DC bus currents.
The five-level CFI is controlled using SVM technique. Both CFI units have identical three-level space vector diagram. A five-level space vector diagram as shown in Fig. 2 is obtained from these three-level space vector diagrams when the DC-bus current of both three-level CFIs is the same. There are 49 redundant switching state vectors which lead to 19 switching state vector positions. Any one of the redundant switching state vectors can be used to realize the reference space vector in a particular sector. CFI DC-link voltages vDC1 and vDC2 toggle between zero and instantaneous line voltages based on switching state of respective three-level CFIs.

Table -1: Classification of the Vectors

Class	Type	Vectors
Class 1	Large vectors	56;56, 16;16, 12;12, 32;32, 34;34, 54;54
Class 2	Medium vectors	16;56, 56;16, 12;16, 16;12, 32;12, 12;32, 32;34, 34;32, 34;54, 54;34, 54;56, 56;54
Class 3	Small vectors	56;52, 52;56, 56;36, 36;56, 54;16, 16;54, 16;14, 14;16, 16;36, 36;16, 56;12, 12;56, 32;36, 36;32, 32;52, 52;32, 12;34, 34;12, 54;14, 14;54, 54;52, 52;54, 34;56, 56;34
Class 4	Zero vectors	14;36, 36;52, 52;14, 36;14, 52;36, 14;52, 14;14, 36;36, 52;52, 12;54, 54;12, 32;56, 56;32, 34;16, 16;34

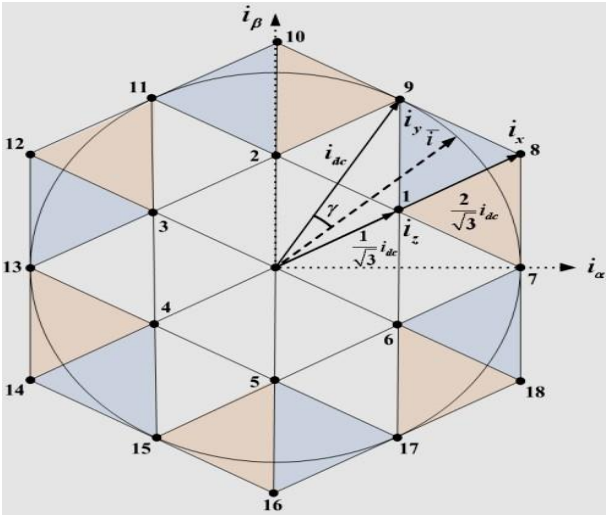


Figure 2: Space Vector Diagram for 5-Level CFI

The current space vectors can be divided into four classes, namely Large, Medium, Small and Zero vectors as shown in Table I. Each switching state is represented by four digits separated by a semicolon, the first two representing two on-state switches in inverter1 and the last two denoting two on-state switches in inverter 2, respectively. In order to balance the dc current between the two inverters, a new switching pattern based onthe space vector modulation is proposed [7].

The key points for designing the new pattern are listed:
1) Small and Zero current vectors are not allowed since they introduce a shoot through condition by turning on the two devices in the same leg, resulting in increased switching frequency and high energy loss.
2) Large vectors cannot be used since they turn on the same devices and do not affect the dc current in the inverters.
3) Only the Medium vectors can be utilized for the dc current balance control. Making use of the redundant switching states for the medium vectors, the dc currents in the two inverters can be controlled independently.

5. 7-Level Current Fed Inverter

A seven-level current-fed inverter (CFI) is powered by a large array of PV-modules. The central five-level CFI is composed of two three-phase, three-level CFI units, each connected to isolated groups of PV modules on the DC side. This power converter system offers several advantages: (a) Each PV module operates at its maximum power point (MPP), even in cases of non-uniform insolation across the PV plant; (b) The system eliminates the need for large energy storage inductors or capacitors on the DC side of the five-level CFI; and (c) The required small filter for the DC-DC converter and CFI can be realized using a polypropylene film capacitor, which enhances reliability.

This power converter system configuration can be further expanded in a modular manner. For instance, a third three-level CFI unit can be added in parallel with the existing two three-level CFI units on the AC side. A new section of PV modules would then be connected to the DC bus of this additional CFI. Together, these three CFI units operate as a single seven-level inverter. In this chapter, a seven-level space vector diagram is shown in fig.3, developed to facilitate the implementation of the space vector modulation (SVM) technique. A seven-level output current waveform is achieved when the DC bus currents of all CFI units are of equal magnitude.

In this paper explores the comparative benefits of the seven-level current-fed converter over the five-level converter, with a particular focus on waveform quality and harmonic distortion. The seven-level converter is designed to generate an output waveform with seven discrete current levels, which allows for a finer approximation of the desired sinusoidal waveform. This increased number of levels contributes to a reduction in the harmonic content present in the output voltage and current.

The key to achieving a lower THD with the seven-level converter lies in the advanced modulation techniques employed. By utilizing Space Vector Pulse Width Modulation (SVPWM) and carefully selecting the switching state vectors, the seven-level converter can minimize low-frequency pulsations and harmonics more effectively than the five-level converter. The improved time-sharing among switching state vectors in the seven-level configuration helps in smoothing the output waveform, thereby reducing the harmonic distortion.

Table 2 categorizes current space vectors into six distinct types based on their switching state vector positions and the number of possible combinations available for each type. For example, Type-1 includes six switching state vectors (I1 to I6) with 24 possible combinations, allowing for moderate operational flexibility. In contrast, Type-5, which contains vectors like I_{20}, I_{23}, and others, has only one possible combination, reflecting its use in very specific or critical conditions within the power conversion system.

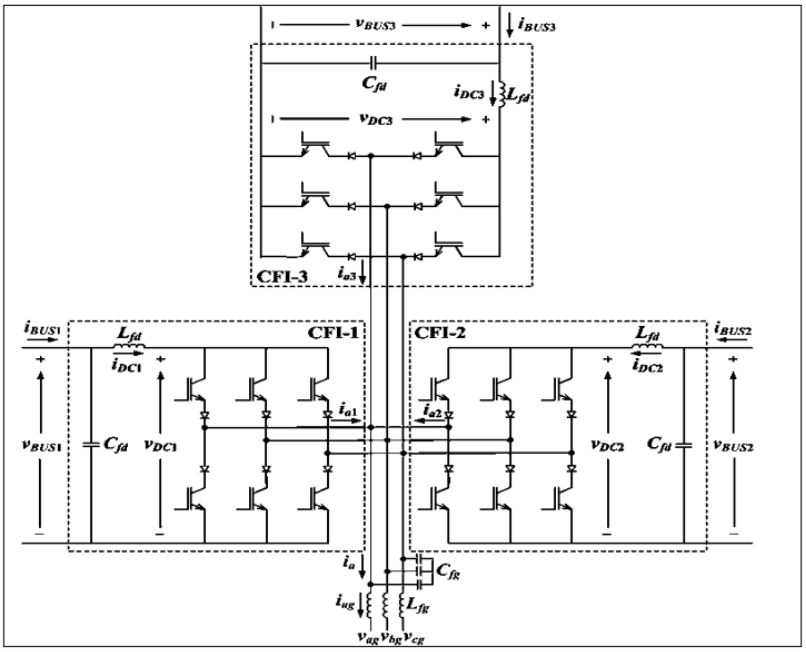


Figure 3: Seven Level Current Fed Inverter

This classification helps in understanding the different roles and flexibility of each vector type in achieving desired current waveforms in multilevel inverters.

Table 2: Classification of Current Space Vectors

Type	Switching State Vector Positions	Number of Possible Combinations
Type-0	I_0	31
Type- 1	$I_1, I_2, I_3, I_4, I_5, I_6$	24
Type-2	$I_7, I_9, I_{11}, I_{13}, I_{15}, I_{17}$	12
Type-3	$I_8, I_{10}, I_{12}, I_{14}, I_{16}, I_{18}$	9
Type-4	$I_{19}, I_{21}, I_{22}, I_{24}, I_{25}, I_{27}, I_{28}, I_{30}, I_{31}, I_{33}, I_{34}, I_{36}$	3
Type-5	$I_{20}, I_{23}, I_{26}, I_{29}, I_{32}, I_{35}$	1

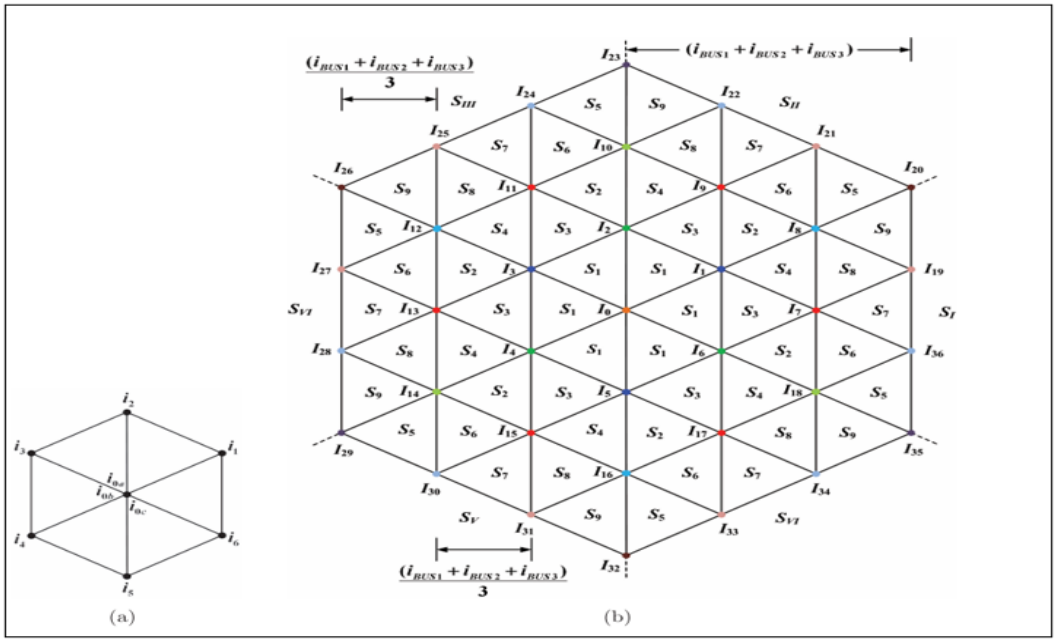


Figure 4: (a) Three-level Space Vector Diagram of CFI units (b) Seven-level Space Vector Diagram.

The seven level space vector is a complex diagram is divided into six major sectors (SI to SVI), with each major sector further subdivided into nine minor sectors (S1 to S9), as illustrated in Fig. 4. Various vectors (I_1 through I_{36}) are placed at the vertices of the triangles, with boundaries between the sectors defined by these vectors. The positions of these vectors likely correspond to specific switching states in a converter. Selecting specific switching state vectors to achieve desired current levels in each sector, reducing distortion in grid currents.

6. Simulation Results

5 & 7 level Current fed Inverters are simulated by using MATLAB by considering Inverter parameters in table 3 & PV module parameters in table 4.

Table 3: Current Fed Inverter Parameters

Rated Power	150KVA
Grid Line Voltage, Vg	415V
AC Filter Inductor, Lfg	0.6mH
AC Filter capacitor, Cfg	150µF
DC bus filter inductor, Lfd	5mH
DC bus filter capacitor, Cfd	150µF
Switching frequency, fsw	1.8kHz

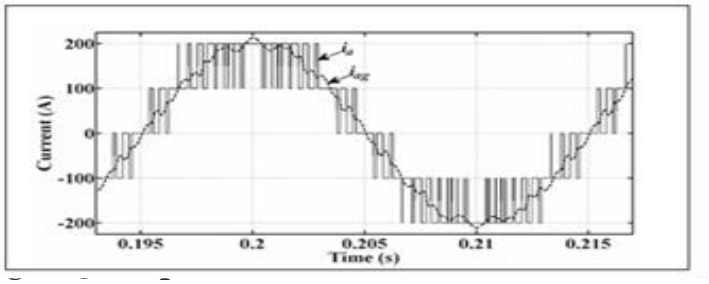
Table 4: PV Module Parameters

Maximum Power	7.5W

Open Circuit Voltage, Voc	12.5V
Short Circuit Current, Isc	20.6A
Reference Temperature	25°C
Reference Irradiance	1000W/m²

6.1 5-Level Current Fed Inverter

Five-level output currents of combined control of inverters at fundamental frequency (50 Hz). Five level output phase a current is 210.9A. shown in fig 5.



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DC-link voltage has ripple frequency harmonic component at 300 Hz which can be eliminated by placing a LC-filter at the DC-side. Average value or dc value of the DC-link voltage (V_{DC}) is around 555 V the results are same for both the dc-link voltages. $V_{DC1} = V_{DC2} = V_{DC}$. Shown in figures 6&7.

The harmonic spectrum of converter output current is shown in figure 8 indicates THD 12.39% and grid current shown in figure 9 indicates a low level of distortion in the output signal, with a Total Harmonic Distortion (THD) of 3.10%.

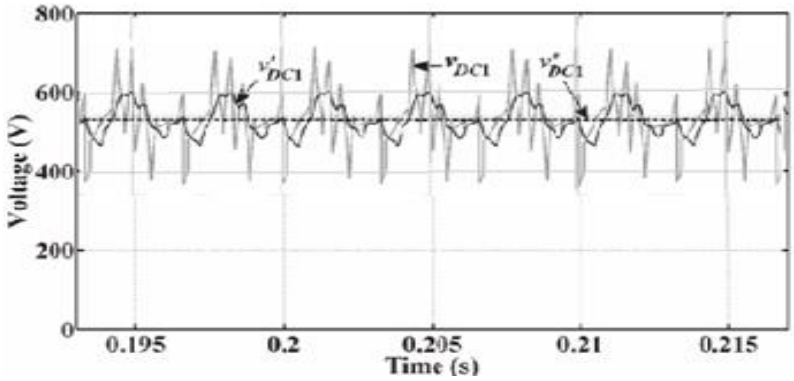

Figure 6: DC Link Voltage of CFI 1

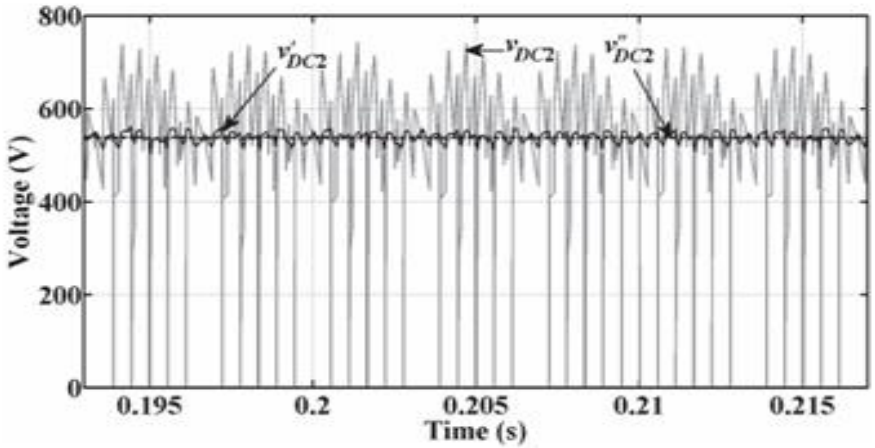

Figure 7: DC Link Voltage of CFI 2

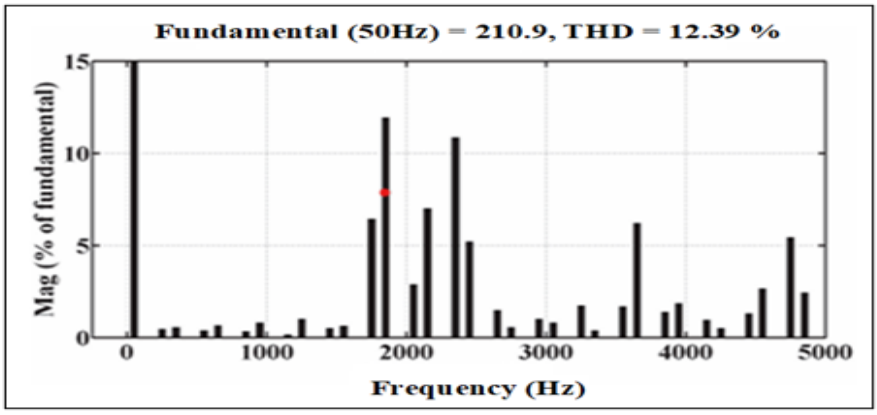

Figure 8: FFT Analysis of Out Put Converter

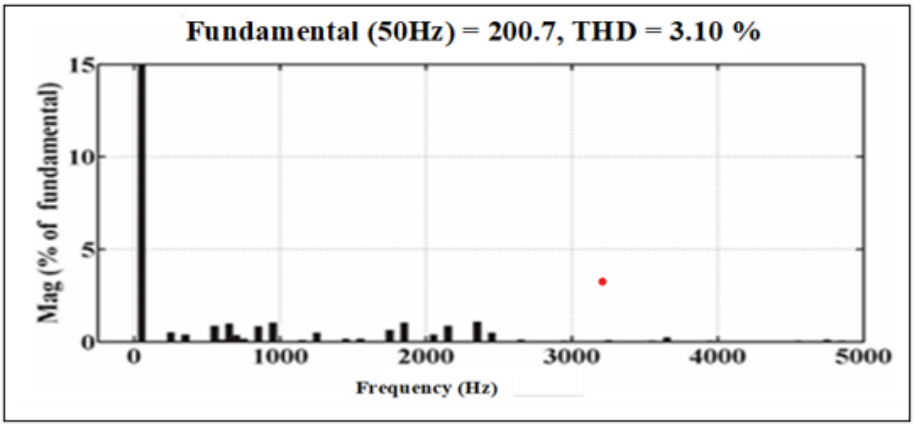

Figure 9: FFT Analysis of Grid Current

6.2 7-Level Current Fed Inverter

The 7-level configuration with equal DC link currents, the converter output current 295.5A is shown in fig 10 and grid current is 287.2A.

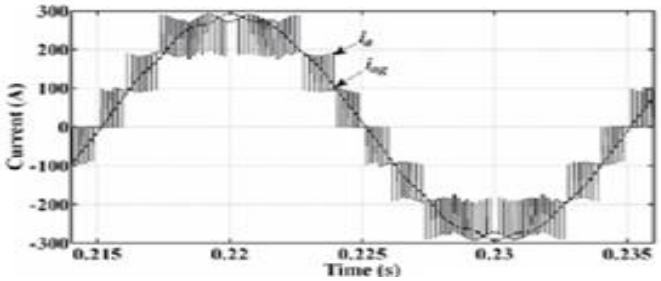

Figure 10: Output and Grid Current

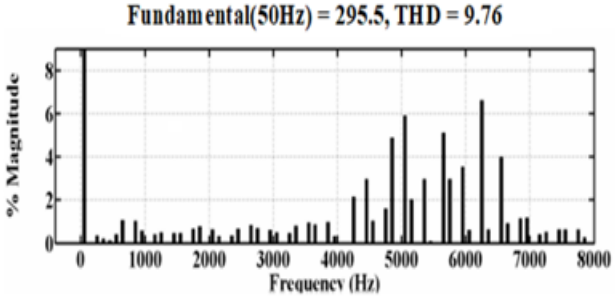

Figure 11: FFT Analysis of Out put Current

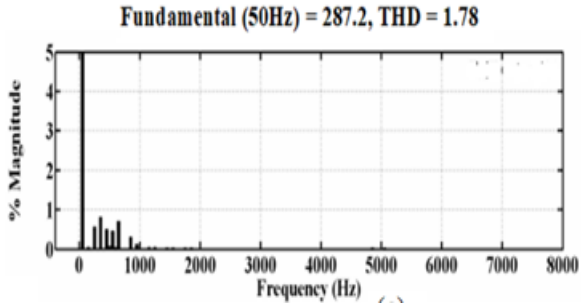

Figure 12: FFT Analysis of Grid Current

The converter and grid THD values of 7-level converter is shown in fig11 & 12 at 9.76% & 1.78% respectively. The DC link voltage remains stable at 555V is shown in fig 13.

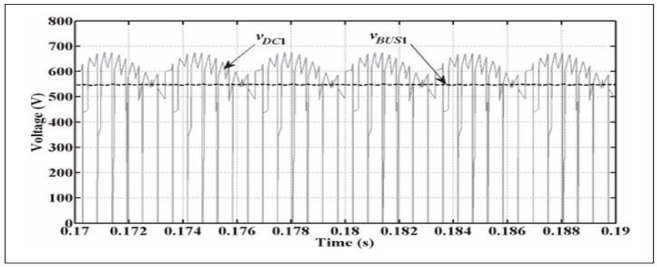

Figure 13: DC Link Voltage of CFI 1

Table 5: Comparison Results

	Ia	Iag	THD		DC Link Voltage
			Ia	Iag	
5-Level CFI (Idc1= Idc2=100A)	210.9	200.7	12.39	3.10	555V
7-Level CFI (Idc1= Idc2= Idc3= 100A)	295.5	287.2	9.76	1.78	555V

In the 7-level configuration with equal DC link currents, the current values are the highest among all cases, and the THD is the lowest at 9.76%. The DC link voltage remains stable at 555V shown in table 5, indicating improved performance with more levels and equal currents.

6. CONCLUSIONS

The multilevel current fed inverters in photovoltaic (PV) systems have been well-suited in power systems due to their numerous advantages. A greater number of levels in a multilevel inverter typically leads to enhanced performance. The 7-level multilevel inverter performance is better than the 5-level inverter in terms of power factor, total harmonic distortion (THD), and overall efficiency. Furthermore, the 7-level inverter is more suitable for grid connected PV plant.

REFERENCES

[1] M. P. Aguirre, L. Calvino and M. I. Valla, "Multilevel Current-Source Inverter with FPGA Control," IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 3-10, Jan. 2013.
[2] N. Binesh and B. Wu, "5-level parallel current source inverter for high power application with DC current balance control," in Proc. IEEE Int. Electric Machines and Drives Conf. (IEMDC), 2011, pp. 504-509.
[3] M. Brenna, R. Faranda and S. Leva, "Dynamic analysis of a new network topology for high power grid connected PV systems," in Proc. IEEE Power and Energy Soc. General Meeting, 2010, pp. 1-7.
[4] D. Xu†, N.R. Zargari*, B. Wu†, J. Wiseman*, B. Yuwen† and S. Rizzo*, "A Medium Voltage AC Drive with Parallel Current Source Inverters for High Power Applications" 0-7803-9033-4/05/$20.00 ©2005 IEEE.
[5] P. P. Dash and M. Kazerani, "Harmonic elimination in a multilevel current-source inverter-based grid-connected photovoltaic system," in Proc. IEEE Ind. Electron. Soc. Conf. (IECON), 2012, pp. 1001-1006.
[6] L. Bangyin, D. Shanxu and C. Tao, "Photovoltaic DC-building-module-based BIPV system-concept and design considerations," IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1418-1429, May 2011

[7] S. Jian and W. L. Yun, “A space-vector modulation method for common-mode voltage reduction in current-source converters,” IEEE Trans. Power Electron., vol. 29, no. 1, pp. 374–385, Jan. 2014.
[8] M. C. Chandorkar, D. M. Divan and R. H. Lasseter, "Control techniques for multiple current source GTO converters," IEEE Trans. Ind. Appl., vol. 31, no. I, pp. 134-140, Jan. 1995.
[9] B. Zhihong, Z. Zhongchao and Z. Yao, "A generalized three-phase multilevel current source inverter with carrier phase-shifted SPWM," Proc. IEEE Power Electron. Specialists Con! pp. 2055-2060, June 2007
[10] B. S. Dupczak, A. J. Perin, and M. L. Heldwein, “Space vector modulation strategy applied to inter-phase transformers-based five-level current source inverters,” IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2740–2751, Jun. 2012.
[11] Shang and Y. W. Li, “A space-vector modulation method for common-mode voltage reduction in current-source converters,” IEEE Transactions on power electronics, vol. 29, no. 1, pp. 374–385, 2013

BIOGRAPHIES

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