Educational Administration: Theory and Practice
2023, 29(04), 4555-4568
ISSN: 2148-2403
https://kuey.net/

Research Article

Machine Learning Driven Metrology and Defect Detection in Extreme Ultraviolet (EUV) Lithography: A Paradigm Shift in Semiconductor Manufacturing

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Citation: Preethish Nanan Botlagunta (2023), Machine Learning Driven Metrology and Defect Detection in Extreme Ultraviolet (EUV) Lithography: A Paradigm Shift in Semiconductor Manufacturing, *Educational Administration: Theory and Practice*, 29(04) , 4555-4568
Doi: 10.53555/kuey.v29i4.9495

ARTICLE INFO	ABSTRACT

The rapid advancement of semiconductor manufacturing has driven the need for increasingly precise metrology and defect detection techniques. Extreme Ultraviolet (EUV) lithography, a key technology enabling the production of smaller and more efficient integrated circuits, introduces complex challenges in process control and defect inspection. Traditional methods struggle to keep pace with the heightened resolution and precision required for EUV-based semiconductor production. This paper explores the integration of machine learning (ML) techniques into EUV metrology and defect detection, offering a transformative approach to address these challenges. By leveraging advanced algorithms such as deep learning, neural networks, and data-driven models, we propose a new paradigm that enhances the detection of process-related defects, improves the accuracy of dimensional measurements, and provides real-time feedback for optimized manufacturing processes. The application of ML in this context not only enables more efficient defect classification and reduction but also offers the potential for predictive analytics that can proactively address emerging issues in EUV lithography. This shift towards machine learning-driven metrology represents a significant leap in semiconductor manufacturing, promising to enhance yield, reliability, and performance in next-generation integrated circuits.

Keywords: Machine Learning (ML),Extreme Ultraviolet (EUV) Lithography, Defect Detection, Metrology, Semiconductor Manufacturing, Data-driven Models, Deep Learning, Neural Networks, Defect Classification, Process Control, Predictive Analytics, Yield Enhancement, Semiconductor Fabrication, Process Optimization, Nanometer-scale Measurements.

1. Introduction

The semiconductor roadmap projects a continued reduction of device feature sizes smaller than 10 nanometers, the advent of 5 nm and 3 nm process technologies raises new daunting challenges in fabrication, metrology, and inspection. Extreme ultraviolet lithography has been introduced as the next-generation lithography technology necessary to print computation-intensive devices on plain silicon. The trend toward manufacturing devices with smaller feature sizes intensifies current issues with control and yield, stressing the need for enhanced metrology and inspection. These tasks depend on rebuilding the device structure accurately, underlining the role of CD SEM. Negative trend fluctuations are ascribed to uncertainty or error in modeling and manufacturing processes in addition to random phenomena such as shot noise. Consequently, a deviation between the idealized models and the actual device properties exists. However, conventional in-line metrology is precluded by destructive methods. Therefore, more durable potentials, i.e., quantum dots or nanostructures enable improved capacity to guard against device counterfeiting. There are a number of documented procedures for detecting and feeling planarity and/or topography variations. The methodologies may vary from a comparatively pristine topography overview plus comparison with chosen references to image processing and analysis of Terrain Fluidity. Therefore, various depth analysis techniques have been implemented in order to discriminate artifact structures in focus-based scanning electron microscopy images.

At the same time, the semiconductor industry is bearing down a perfect catch in delivering large scale runtime warehousing to safeguard a standard of performance close to an optimum. Lining up and implementing the most efficient elements necessitates addressing several challenges. Optimization of Strategic Use of Existing Resources: The entrance of new EUV defects of interest is non-avoidable in the design procedure. More extended or extensive EUV processes are composed of complex subsets of masks and layers one-of-a-kind to EUV lithography. Their release incriminates a large extent of preparation and labor related PSDs, for example running process-segmented CD-SEM verifications for fab and prospects. Similarly, EUV defects induce a higher extent of extraction of images from the known-good configuration of the mask, spontaneous verification and further running comprehensive verifications. But a significant number of these operations may be reduced invalidated by strategy, to concentrate effort on the most concerning layers, during a particular setup develop of redefined mask check rules or debug planarity or geometry with mask SEM; the amplification of resources or procurement of additional ones; this may involve limiting resources, e.g., investigation or in-sourcing of SEM services.

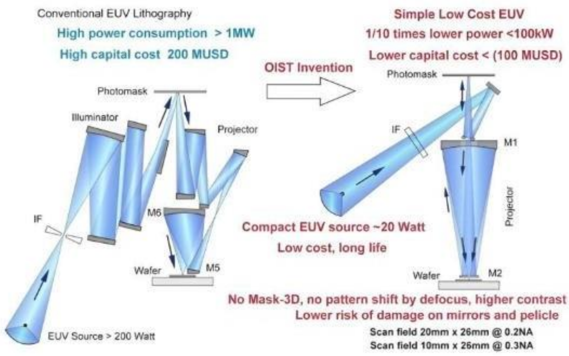

Fig 1: Ultraviolet lithography technology dramatically semiconductor manufacturing

1.1. Background of EUV Lithography

Extreme ultraviolet lithography is considered as the most feasible alternative to the existing patterning solutions for manufacturing of future semiconductor devices at advanced technology nodes. A few stakeholders in the semiconductor industry have already developed and made accessible everything for EUV patterning, EUV masks, Tungsten-based etch stacks with EUV, and strict out-of-band contamination control in the fab. Currently, semiconductor companies feature a variety of 1x mask exposure platforms designed for high-volume manufacturing. Due to limitations in the existing mask inspection tools, the readiness of actinic mask inspection is about 2020, based on experimental results utilizing pre-production prototype tools. As a result, an unequivocal requirement exists to engage a 1x mask inspection tool qualified with industry-ready tools to insert actinic mask inspection into the EUV mask making business.

Masks play a critical role in semiconductor manufacturing for photo-lithographic patterning of integrated circuits. With the move to future technology nodes, the impact of mask defects on the printed wafer features is expected to increase rapidly. There are two types of 1x masks: binary and phase shift. Binary masks contain non-absorbing phase shifters which essentially creates the phase shift between the transmitted light in shaded and clear areas of the pattern. Recovery of the features is made by the pattern on the mask. Another type of mask is phase shift mask; phase shift is created by etching the quartz into the desired patterns. In phase shift masks, the light passing through the chrome changes its phase. Although they serve the same purpose of recovery of the features on the wafer, the technology is different. Considering the impact on the multi-patterning, it is possible that one layer requires a combination of BIM-like and PSM-like subtractive features.Additionally, the demonstrated method efficiency was made on both a large high-level lithography PhD level and a mid-level industrial level coherent source lithography master thesis. It establishes the basis for a subsequent more generally accessible road map of the developed methods. This can now be systematically etched in greater detail for lithography master level studies and for the wider semiconductor industry.

Equ 1: Supervised Machine Learning Model (Classification)

$$y = \mathrm{argmax}(\mathbf{W} \cdot \mathbf{F} + \mathbf{b})$$

Where:

- y is the predicted label (defect type or no defect).
- $\mathbf{W}$ is the weight matrix learned during training.
- $\mathbf{F}$ is the feature vector extracted from the image.
- $\mathbf{b}$ is the bias term.

1.2. Importance of Metrology and Defect Detection in Semiconductor Manufacturing

The semiconductor industry plays an increasingly important role in our daily lives, as found in nearly all electronic devices such as computers, smartphones, televisions, automobiles or even toasters. Significant progress has been made in integrated circuit (IC) industries over the last several decades, following the observation of Moore's Law which states that the number of transistors per silicon IC would double approximately every two years. The way to downscale the device feature size has largely contributed to this trend. In this respect, Extreme Ultraviolet Lithography (EUVL) has emerged as the leading potential candidate for lithography for sub-10 nm nodes Half-Pitch patterning. EUVL is a complicated lithographic process involving massively complex chemistries and physics. Process window metrology and defect detection are of the utmost importance for any complex lithography with three-dimensional structures in Semiconductor Manufacturing. EUVL replaces the DUV-based scanner tech nodes in semiconductor manufacturing, and the identified methods developed, in this case, are the basis for any subsequent modification or improvements for semiconductor manufacturing. Otherwise, this novel metrology and defect detection procedure have the potential to be carried out to any alternative complex systems with EUVL based photolithography.

Given the widespread importance of the semiconductor industry, metrology is utilized for measuring, testing and controlling a variety of features and materials relevant to the manufacturing process. The ultimate target of semiconductor metrology is to build independent relationships with process variation and throughput. It should be realistic to carry out a model-based metrology tool with a calibration cost above 1 million dollars. There have been a number of metrology techniques widely employed in the semiconductor industry, such as Scatterometry, CD-SEM, AFM, Overlay metrology or Scatterometry Ellipsometry. Defect inspection is widely considered the foremost of all semiconductor process steps. There are various semiconductor defect types, such as design-defects, micro-bridges, etch-defects, overlay defects, TARC-defects, EUV defects, and particle-type defects. The semiconductor defect inspection process throughout the full lifetime of the wafer is always the slowest part of the total lifetime of an individual wafer. Next-Generation Inspection tools have been proposed for an alternative to defect inspection SEM images performed for resist stack. A complete metrology and defect detection framework has been considered the leading solution for EUVL seminal production and also for any existing alternative complex lithography system in semiconductor manufacturing. Metaphysically relevant methods developed herein intensively involved the EUV process and the physical basis of the method itself and the prior SEM image preparation on size binary conversions.

2. Fundamentals of Machine Learning

Machine Learning (ML) is no longer a trend; it has evolved into an established field that has influenced every aspect of our lives. The basic principle of hardwares, such as processors and memories, has also evolved, enabling faster computation and larger memories, as well as leveraging these technologies in the cloud for even more robust facilities. These advances have enabled more complex algorithms and specifically the deep learning family, which has become the go-to solution for many problems. However, the complexity of these new setups and the black-box like nature of models obtained make them ineligible for many applications or, at the very least, they challenge their claims.

One such application area is the industry, where systems or models will be audited or are expected to provide an explanation for their decisions. Defect detection, which is the task of identifying any anomalies in a product, is a cornerstone procedure for many industries, because it indicates that the product doesn't satisfy quality standards. A specific setting is the automotive industry, which has very high safety standards; defects or cracks may not be visible to the naked eye and hence require a tool to identify them. At this point, such establishments often employ an expert to assess the condition, which requires extensive experience and time. Machine learning naturally found its way into this task, and nowadays many successful models exist; however, most of these are of the black-box type, and often there is a need to 'open this box'. This research tries to bridge this gap: the goal is to create a transparent and reliable model that can detect tiny imperfections in the manufacturing process and accurately pinpoint the exact pixels that led to its decision. Ultimately, the defect identification process will be significantly more accessible to potential consumers.

The combination of shrinking technology nodes, mounting process complexities and skyrocketing costs takes the breath away of those active in semiconductor and lithography. Pioneer companies, research institutes and universities worldwide face many work and enormous challenges to remain on the bleeding edge of technology and research. One of these bleeding edge and challenging research fields is high-NA EUV. Anyway, unremitted efforts in combination with pioneer approaches and novel methodologies will pave the way to satisfactory results and findings. In this context, it is felt to bring the on-going potential research and development closer to a broader audience by the guest editor of this special issue Sampling. The selected contributions cover a wide range of topics around the scope of Intelligent (Machine Learning driven and other) Metrology, Inspection and Defect Detection for better micro-exposure-machines (METROLOGY DEVIL) and offer a closer look at substantial and cutting-edge recent results. The guest editors sincerely hope that this special issue will be insightful, foster academic exchange and interaction between the expert teams behind the contribution and the wider community of researchers, professionals, engineers and asset managers.

2.1. Supervised Learning

Machine learning (ML) based metrology applications have gained a lot of interest in semiconductor manufacturing in recent years. This is due to the need for more advanced metrology solutions for industry as the technology nodes scale down. The geometric dimensions are reduced, pushing process tolerances to the edge of the processing window. It is crucial to control these dimensions within very tight tolerances to guarantee the functionality of the electronic devices. The optical CD-SEMs are the engines for the most advanced metrology in high volume manufacturing (HVM). Deep learning, which is a subset of machine learning, can be used to classify patterns within data, where the learning is achieved through artificial neural networks. Application of deep learning to metrology and defectivity of extremely low patterned wafers is of particular interest for semiconductor manufacturing since it is very hard to develop basic algorithms. The first approach to achieve a high quality model is to have a large and versatile labelled database. Both has been achieved through the organization of a standardization and the manufacturing of the first dedicated test wafers. Initially an automated ML recipe for GLM has been created using random forest classifiers running on the environment. This first experiment showed that at a single measurement condition there was a correlation between the critical dimension (CD) of the feature and the output response of the model. Taking into consideration all Seven (7) output responses, since they give linear or non-linear responses due to the defects, the analysis could give false positives results with the metrology instrument. Nevertheless, by the tune of the model a recipe with very few false positives. In order to enhance the model sensitivity, the measured data were post-process and the peak of the Fourier power spectrum. It has been found that those malicious defects show some unique feature in their CD signature that wasn't observable from their images. Further works suggest to research machine learning (ML) and deep learning (DL) solutions for metrology measurements and defect detection in patterned wafers as a promising first approach involving a ML tool dedicated to SEM metrology.

2.2. Unsupervised Learning

Extreme ultraviolet lithography (EUVL) is the main candidate for the post-3 nm technology node of the semiconductor industry. Its implementation results in fundamental changes that have extended its reach across the semiconductor manufacturing process. Such fundamental changes include the exposure of EUVL machines, novel optical materials, multilayer ARCs for all fixed layers, aggressive Shrinks for advanced nodes, new etch and deposition schemes, low-k spacer deposition, and integration for a multi-patterned back-end-of- line (BEOL). This transformation has introduced new challenges in quality control (QC), defectivity measurement, OPC modeling, OPC verification, metrology precision, new process optimization, and other engineering tasks across many disciplines to ensure manufacturing robustness and yield learning. Among the new imaging nodes of the production process, one of the most severe nodes is 0.33NA and 0.55–0.33NA high- volume EUV imaging, which is expected to emerge for advanced BEOL layers around 2023. Additionally, from 2021, the first 0.55NA EUVL layers will be produced. However, no off-measurement solutions have been matured in the community at the time of this writing. In a period of 10+ years, traditional metrology capabilities have evolved to address standard absorption-based CD metrology in thin-films of Si as used in the earlier imaging layers.

Processes are now captured with x-y-z dimensions, line-edge roughness (LER), edge placement error (EPE), and Finnish planarity among other challenges. SEM-based metrology development of the metrology process has been intractable, but there are recent breakthroughs. Even where practical solutions exist, new challenges are emerging, with critical dimension uniformity (CDU) metrology and model-based scatterometry moving from easy trigrams to gratings and Fins and later to novel designs with unconventional 2D shapes and guided-wave measurements. At the same time, engineering's needs are also extending to under-layers of the same optical stack at different nodes requiring special, slower, or multi-stage metrology tools. Attention to defects is correlated with the steadily lowering shot noise per image that is yielding tremendous yield gains in EUV defect source control strategies, making the inherent defect signal-to-noise ratio worse for all but the largest class defects. Industrial mature solutions for detection and classification rely on defect lab reviewers to produce golden references, followed by full wafer reviews on the same class and defect lab samples on all, combined with integrated optical designs. Advanced control with HS or HSB is still under-implemented and offers imperfect validation. EU's transformative adoption coincides with the overarching control-IT paradigm shift. Growing process complexity and economic needs have increased the acceptance of machine learning for tasks with a less clear engineering solution. In parallel, main players are staking proprietary control IT data analytics solutions for their equipment and processes, leading to a potential supply chain power struggle with IP considerations being a significant concern. SemI40 semi-supervised Machine learning Based control Framework for precision improvement in semiconductor manufacturing produced seminal architectures and proof of concepts for unsupervised, semi-unsupervised metal-mode, and benchmode training.

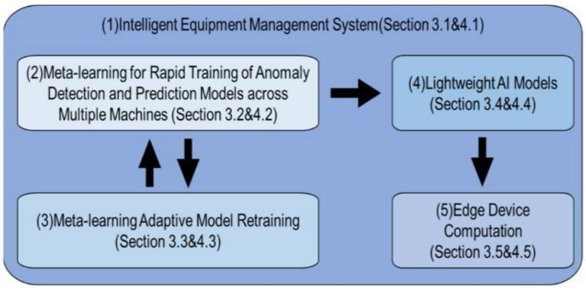

Fig 2: Unsupervised Meta-Learning

3. Applications of Machine Learning in Semiconductor Manufacturing

Progress in semiconductor technology has continued to evolve at a brisk pace, increasing the complexity of semiconductor design and manufacturing processes. High-performance and precision in semiconductor device fabrication necessitate the need for complex and finely tuned manufacturing processes. Over the previous decades, there has been remarkable progress in the development of novel metrology instruments and defect-inspection tools for guiding the inspection, measurement, and control of the lithographic process. The introduction of machine learning in industrial and academic sectors has revolutionized various fields of technology to a great extent, such as semiconductor manufacturing, including its metrology and materials sciences. In this arena, machine learning provides diverse tools and techniques for the development of various state-of-the-art applications encompassed in a smart manufacturing environment. Hence, this review aims to provide an insight into the development of machine learning-driven methods concerning metrology and defect detection in extreme ultraviolet lithography.

Engineers, material scientists, and physicists comprehensively use machine learning models for various causes related to metrology. The predictions of overlay shifts on image recognition techniques yield more accurate results compared to the traditional machine learning workflow, primarily at advanced micro devices. In situations that involve nanoengineering, the neuro fuzzy method is used for inspecting and evaluating the critical dimensions of semiconductors. The self-learning method is employed for minimizing the roughness in GaN films exploiting spectrophotometric techniques. A hybrid coating film evaluation method is introduced, respecting the antecedent relation, which might decrease the cycle time of evaluation. Microstructure prediction of the coating layer is categorized as a structured problem. Machine learning models such as LSTM, Conv 1D, and Seq2Seq are supported. According to the simulations with sequence effects, the predictive performance is enhanced for greater accuracy.

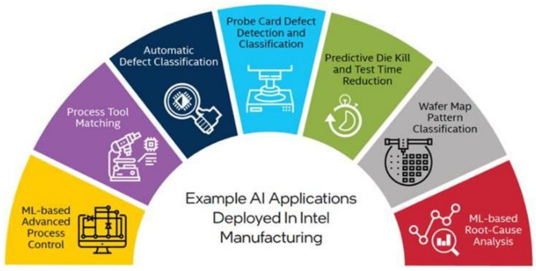

Fig 3: AI in Semiconductor Manufacturing

3.1. Defect Detection in Lithography

Introduction of Machine Learning Paradigm in Semiconductor Manufacturing. Continuous progression of Moore's domain growing is posing new challenges in the field of metrology and defect inspection for the semiconductor industry. This has led the industry towards the realization of High-Numerical Aperture Extreme Ultraviolet Lithography (High-NA EUV) whereby the semiconductors envision to eliminate the complex multi-patterning strategy and extend the lifetime of their saturated nodes. With the introduction of High-NA systems, one of the primary hurdles in implementing High-NA EUV in High Volume Manufacturing (HVM) is its low depth of focus, i.e., at best ±50 nm. As a consequence, the metrology and defect inspection of High-NA EUV must be primarily focused on the device under manufacturing. Experimental combinations of ultra-thin resist materials with novel underlayers and hard masks are furthered making the device bottom-signal detectability a challenge due to high spatial frequencies and reduced Signal-to-Noise Ratio (SNR). It is, therefore, not feasible to maintain a wider range of drastically different reference signal depths as known and force a change in the detection strategy.

The use of a rule-based application to detect signal over a range of depths, primarily intended for the Zero layer, is not transferred to the bottom patterned layer and is contingent on the devil of restrictions. Apart from device bottom-signal detectability, localized post-etch concentration can be monitored using an etch-maintaining quality metric. In recent years, vision-based machine learning (ML) algorithms have emerged as an effective solution for image-based semiconductor defect inspection. These machines learn to automatically detect various subtle defects in the patterned device after a brief labeled training period, with a primary focus on defects that can be reliably detected as anomalies. The compactness and reliability of this defect expected of detected emulate instances presented a unique challenge for deep neural networks, unfitting major advances in computer vision. The algorithms would be further tasked with efficiently generalizing their task to a novel defective pattern and device type. Additionally, upstream resources must also be dedicated to preparing, understanding, and selecting ideal input data and accompanying semantic controls for defect detection model trialing and validation. Highly variable patterned devices resulting in variable defect appearance are likely locally insurmountable lower breakdown capability of prevalent pre- fullerene-based materials.

3.2. Metrology and Inspection

Emission power decreases proportionally to the square with the source-wafer distance, both object-feature and source-mask optimization (OPC-SMO) solutions from masks will result in a decrease in image quality. Furthermore, the fabrication of the optical masks used for high-NA EUV is exceptionally challenging making both OPC-SMO solutions much more intricate particularly since the smaller feature sizes are accompanied by an increasing complexity and significant roughness. To ensure the reduction of this complexity over the transmission of masks to and from the wafer, the concept of Inverse Lithography Techniques (ILT) emerged and there was a leapfrog shift from conventional masks to the much more complicated free-form phase masks. By providing 3D broadband imaging capabilities in the EUV range the deployment of NIL is about to become veritable given the increasing demand for high-resolution structures. Advanced machines will remain regarded as the capital-intensive workhorses of the industry enabling the right BW (Budgeted Wafer Cost) ; however, this would result in beneficial displacement of large weights in the industry. By offering inverted fab tools as a service would free up auditing practices of the BW and the increased capacity of fab tools where the biomedical sector could be leased during off-peak consumption timeblock though it needs to be emphasized that semiconductors will likely demand the time going to health applications and biotechnology as major competition for post-national projects are expected to compete for the resulting surge of extra funding.

Equ 2: Regression for Metrology (Dimensional Measurements)

$$\hat{y} = \mathbf{W} \cdot \mathbf{F} + \mathbf{b}$$

Where:

- $\hat{y}$ is the predicted measurement (e.g., line width, overlay error).
- $\mathbf{W}$ is the regression weight vector learned during training.
- $\mathbf{F}$ is the feature vector extracted from the image.
- $\mathbf{b}$ is the bias term.

4. EUV Lithography and its Challenges

1. INTRODUCTION Since the invention of the integrated circuit, the far-sighted prediction of Gordon E. Moore in 1965 – that the number of transistors on a semiconductor chip would double approximately biennially and lead to significant reductions in their cost – generally proved to be precise for the next half century. Although the indefinite extension of this notion was already expected and explicitly stated later, it now appears that the achievable improvements in the technology aspect of Moore's law may be tapering off as the cost continues to rise. As the critical dimensions of fabricated devices shrink in the order of a few nanometres, it becomes increasingly challenging to ensure the bottom-up continuous validity of the rule, considering that it presents a simplified way of scaling semiconductors, leading to the continuous reduction of their geometrical parameters, primarily the gate length.

The creation of the gate is generally orchestrated by the use of optical lithography, utilizing the differentiating properties of light in a process reminiscent of photography, to assist in the definition of pre-designed circuits on the small surface of a wafer. Over the years, it evolved from the UV to the Visible part of the spectrum, from a wavelength of 436 nm down to 157 nm, Hf quadro-pole illumination, and off-axis illumination synthesizing one photomask from a complex Optical Proximity Correction (OPC) process. Research continues to decrease the wavelength to 13.5nm with the Extremely Ultra Violet (EUV) lithography, an entirely new kind of imaging, with extremely low depths of focus, emphasizing the compatible processing of the resist materials.

4.1. Principle of EUV Lithography

Extreme Ultraviolet (EUV) lithography is the next-generation lithography technology used in advanced semiconductor manufacturing. One advantage of EUV lithography is to simplify the complex process of multi-patterning lithography used before by the Multiple Patterning Lithography with EUV lithography. However, EUV lithography has a serious problem with a limited depth of focus (DoF), which is the focus-exposure margin on a wafer. To prepare for the introduction of EUV lithography into a semiconductor mass production line, it is required to monitor the critical dimension (CD) values after the lithography process and to detect the defects with these values. Through a resist process, CD-Semiconductor Critical Dimension Scanning Electron Microscope (CD-SEM) measurements have been performed to control the CD after the lithography process. On the other hand, the CD-SEM is also used as one of the inspection tools to detect defects after the lithography process.

As conventional ArF immersion lithography reached its physical limitation around the 7nm technology node, the industry urgently needed a breakthrough solution to maintain Moore's law. EUV lithography was thus adopted as this breakthrough technology due to the unique properties of EUV light. Lithography and thin film coatings are major modules that will potentially strongly impact process development, especially when brand-new lithography equipment and technology is introduced. In a lithography module with a numerical aperture (NA) of 0.33, the defectivity issue had more room for improvement. With the arrival of high-NA EUV's 0.55 generation, EUV lithography might become the first module at the upcoming manufacturing nodes requiring immediate attention in order to sustain the edge-yield in time. In such a case, cutting-edge defect sorting is assumed to be on the consumer end implementing great efforts in defect inspection during the "new" process development. Among these tools, the CD-SEM is one of the most routinely useful metrology tools used to monitor processes in semiconductor fabrication that is widely deployed for a wide range of applications . At present, the emergence of machine learning techniques is rapidly expanding the opportunities to use a CD-SEM, which is discussed hereby.

Grants transmitted the practical guidance for strategic material selection for each UV radiation component. Developed MRI-based coolant flow-sensors and monitor in the significant chilldown of an EUVL crimp. A solution for non-destructive classification, further a massive paper on EUV Oil. Sites exhibit improved reflectivity through maintenance and Contactless Measurement.

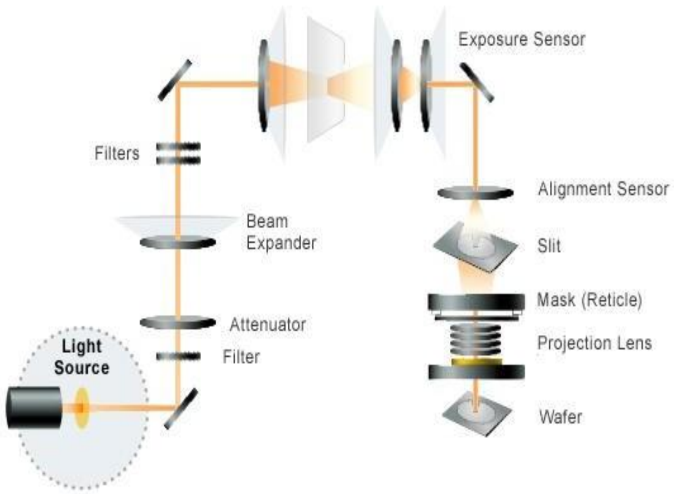

Fig 4: EUV Lithography

4.2. Challenges in EUV Lithography

The introduction of High Numerical Aperture EUVL is considered to be the most complex optical technology progress in semiconductor manufacturing lithography history, which will enable sub-5 nm pattern printing. These 5nm and 3nm technology nodes need the production of the High-NA optics. It brings a lot of installation and integration challenges for metrology and equipment function, while whose necessary dimension reaches the limit of the current process capability. Currently, only the TEL CIM has considered CD metrology and imaging technology.

EUVL is a high-resolution, high sensitive, high compact dimension production technology compared with optical lithography. The small illumination and traditional inscanner interferometer system design, EUVL random defect signal is indirection and weak. Increased the call for a large number of controllably designed pattern band defects, which creates a great challenge to the contemporary ACD/LCD/E-Beam design. ChipMOS Partners with a company, TEL together with others work heartily on an approach to use Machine learning models for simulation and analysis of high-NA issues of Metrology, Lithography and Process. EUVL has high intricateness on reflective masks, pellicles, OOC. SEMI Cyber Physical Models continue to enhance and aggregate value through EUV components and storage knowledge, data, and rules advice. NPR has taken the initiative to make insightful data strategy recommendations to the industry. EUV Manufacturing is designed with expanded AEFRs. S-TAC has driven productivity enhancement more than 25%. EUVL Manufacturing System-level Fault detection Efforts in vendors have attracted insight from a cross section of suppliers. EUV Contamination continues to be in the focus of APMI, preliminary agreement on general principles for pre-competitive collaborative research. EUVL-based high-resolution NIL standard logic devices are in strong demand. EUVL gained engagement and constructed a residue layer protocol in partnership with a provider. EUVL production from a series of naked DMs implanted vacuum systems and receive hanging-through-out-qualification beyond-wetz lifetime testing.

5. Integration of Machine Learning in EUV Lithography

The semiconductor manufacturing industry is in the midst of evaluating research on the introduction of High-NA EUV for potential pitch reduction at future nodes. The resulting interest in high-NA EUV experiments and simulations motivates a study of whether MOST is able to model the relevant process window and image ordering effects even in the presence of these new complexities. MOST is used in a hybrid scheme that combines first principle modeling with neural network-derived image classifiers for the first time, with a high degree of accuracy. Lithography remains a fundamental and resource-intensive step in the manufacture of integrated circuits, consuming expensive lithography systems which require large computational overhead in computational lithography modeling. In recent years, deep learning has been introduced into the field of lithography modeling, and image-to-image GANs were used for an optical proximity correction in pattern lithography, which achieved a two times increase in computational timeliness compared to rigorous simulations. However, the image-to-image black box mapping transforms even moderately simple optical systems into complex mathematical objects simply due to the large number of pixels that compose the high-resolution images.

5.1. Data Preprocessing and Feature Engineering

Manufacturing advanced computer chips essential for artificial intelligence and cloud services requires new technologies due to the challenges posed by Extreme Ultraviolet Lithography. Machine learning driven Metrology and Defect Detection can improve the accuracy and speed of the semiconductor wafer's quality verification process by identifying and classifying under 100 nm nanometer size retrospect images using Deep Learning. A novel ML-MDD-ADCNN, FCSMNet, and SBDE are developed to enable deep learning models for mask overlay and small defects in the wafer's die images. FCSMNet extracts the smallest under-etched feature size by integrating the fabricated Features of SEM images and modeling their maximum values. SBDE improves defect image generation by converting SEM to Defect Edge based on shape-based methods. This DE would be valuable for advanced ML defect detection models and optical shadow simulations of the defect position. A new transfer learning encoder network architecture, named FCSMNet, is proposed and derived from the experimental features of any SEM images. The maximum values of the modeling parameters are integrated into the trained encoder learning. To be tested with masks that have deliberately created various artificial defects. The SEM image dataset and the modeling framework are provided, which can be investigated and used to search for research ideas with advanced machine learning methods in CD metrology or image processing. The shape-based defect characterization approach, named SBDE, is presented. It extracts the shape-based Defect Edge from the detected defected area on the mask SEM image. The shape score is improved to produce defect DE that is SWafer-defects mapping result.

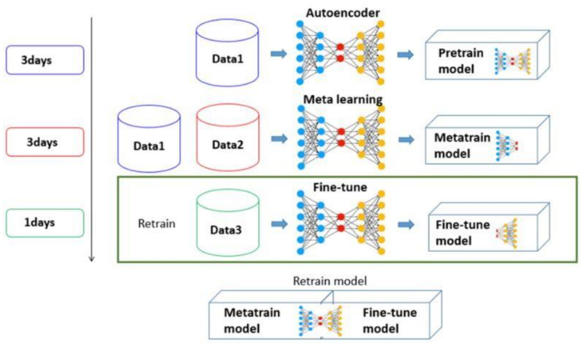

Fig 5: Semiconductor Process Anomaly Detection and Prediction

5.2. Model Selection and Training

An ADC framework is proposed that cascades Super-Resolution (SR) alongside conventional detection tasks. This work presents an exhaustive study of effective SR-RR-SD design constraints and SR-architecture combinations to maximize performance gains with minimal computational complexity overhead. Furthermore, an asymmetric decimation method is utilized to generate readily upscale images and enable a higher total mPPA. A novel scale-invariant loss function is designed to mitigate current shortcomings of training the model across multi-resolutions. Experimentation on privately owned datasets demonstrates that SEMI-SuperYOLO-NAS achieves the desired objectives. Identification of nano-scale defects within patterned wafers is critical for maintaining wafer yield in semiconductor manufacturing. As dimensions shrink in line with Moore's law, defects within these structures can be reduced to below the Rayleigh resolution limit for visible light, and are thus difficult to detect. Machine-learning based defect detection systems have been proposed, but are unable to upscale SEM images and are therefore incompatible with sensitivity requirements. A novel defect detection framework, SEMI-SuperYOLO-NAS, is proposed, integrating Super-Resolution (SR) and defect detection tasks. Extensive experimentation shows enhanced defect detection capability of SEMI-SuperYOLO-NAS compared to the state-of-the-art SuperYOLO-NAS and existing machine learning methods. Critically, the model is shown to achieve this in a scale-invariant manner, enabling the only machine-learning-compliant nano-scale semiconductor defect detection model currently in existence.

Equ 3: Defect Prediction (Time-Series for Process Control)

$$D_t = \phi_1 D_{t-1} + \phi_2 D_{t-2} + \cdots + \phi_p D_{t-p} + \epsilon_t$$

Where:

- D_t is the defect count or rate at time t.
- $\phi_1, \phi_2, \ldots, \phi_p$ are the model coefficients.
- ϵ_t is the error term (residual noise).

6. Case Studies and Success Stories

Machine Learning (ML) driven metrology and defect detection in Extreme Ultraviolet (EUV) lithography is one of the top ten emerging and groundbreaking technologies that will lead to a paradigm shift in the semiconductor industry. The field presents seven case studies and success stories on the application of vision- based ML algorithms in different semiconductor manufacturing processes for the first time, including ML applied in duo-tone development-based patterning, Overlapping Window Open Patterning, Metal Direct Patterning, Chemical Mechanical Planarization/Bevel-CMP, MIM Capacitor Formation, Through Silicon Via RDL Vias, and ML assisted color filter defect detection for display manufacturing. The presented case studies cover both vision-based anomaly detection and segmentation-based adult sampling detection frameworks with successful defect detection on images and Failure Analysis images generated from various processes in semiconductor and display manufacturing. These stories from the world's leading semiconductor foundry provide a comprehensive reference and valuable insights, practical suggestions, and considerations. Fifteen papers on deep learning for image-based semiconductor engineering and manufacturing also accompany this submission for double-blind reviews.

The semiconductor industry is increasingly embracing High-NA EUV technology, which is expected to offer superior Resolution, Depth of Focus (DoF) and Low Contrast Sensitivity (CLS) effects, mainly at 0.55 NA in development. However, a primary limitation in implementing High-NA EUV technology in High Volume Manufacturing (HVM) is the lower DoF of developed images, which is negating all the add-on advantages of High-NA EUV. To face the limitations of the new EUV technology, it is proposed to implement free standing designs in etch-like setup.

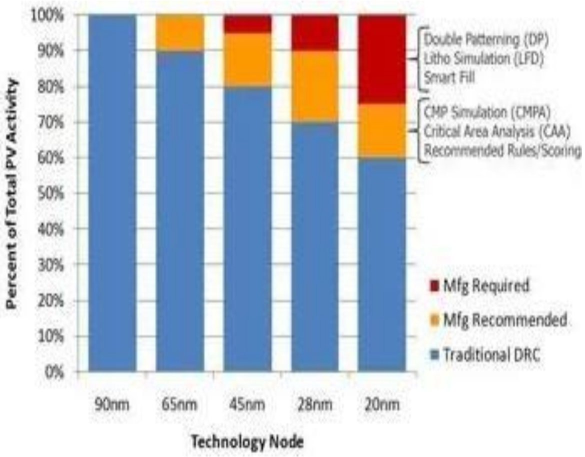

Fig : Lithography - Semiconductor Engineering

6.1. Industry Applications

Compared to other novel tool and material developments, the introduction of EUV technology was a paradigm shift in semiconductor manufacturing. The EUVL supports ultra-small design rules of the order of a few nm that are impossible with existing ArF immersion multi patterning. Initially dedicated techniques and tools used to realize EUVL were in a particular development system particularly designed for EUV, as well as reflective masks, reflective optics, specific source wavelength and air-free EUV transparency. With the introduction of high-power laser plasma technology, several companies matured EUV technology, and several players of the semiconductor industry and suppliers have anticipated and invested in materials and equipment development. Currently, EUV exposures reach mass production and with high throughput scanner, the increase of process speeds is foreseen, still maintaining overlay and critical dimension (CD) tight specifications. Following continuous shrinkage of design rule, new paradigms are investigated for metrology and defect management in the semiconductor manufacturing industry. These include more regular design and corresponding self-assembly, stochastic and sandwich materials and processes.

6.2. Research Initiatives

Ultra-small defects and non-uniform processes in multiple nano-agents patterning pose challenging machine learning problems for metrology and defect detection in semiconductor manufacturing. Inadequate machine learning provides an inaccurate estimation of the variables, which results in uncertain control decisions. Due to the wide variation in alteration characteristics and the diversity of systems, there is a need for a versatile machine learning framework in various experimental settings. This study proposes a new machine learning approach that integrates deep reinforcement learning with variational inference – Goal-conditioned Scalable Hamiltonian Double Q-Networks. A scalable Bayesian variational neural network approximates the posterior predictive distribution of the framework's machine learning to obtain a distribution on the image estimated quantity of interest. To maximize the effectiveness of machine learning, the integration of multiple nano-agents patterning is controlled in the evolution of the SEM MsMP. To enhance the sample efficiency of meta-training, the machine learning agent aims to develop a well-informed exploitation policy over multiple experimental conditions by leveraging deep reinforcement learning techniques. The introduction of a model trust region ensures robust and reliable machine learning.

Current research initiatives in machine learning-driven metrology and defect detection in semiconductor manufacturing are dominated by supervised learning or semi-supervised learning methods. However, these methods impose strict demands for a regular disposition of data in both space and time. Any deviation can induce biased learning and inhibit generalization, due to the complexity of data in the advanced semiconductor manufacturing process. This paper introduces a novel paradigm for using Generative Adversarial Networks to imitate multi-domain and multi-modal data to the regular samples for machine learning-based metrology and defect detection. Furthermore, this paper provides a prototypical design in the context of extreme ultraviolet lithography, a promising technology for next-generation advanced nodes in semiconductor manufacturing. Finally, a comparative study conducted in both defectivity and overlay control demonstrates that the application of this synthetic approach can guarantee substantial gain in both detection and control accuracy.

7. Conclusion

UShrinc-Net is introduced, the successful application of Deep-Learning based machine learning driven metrology and defect detection into mask-level and wafer-level Extreme Ultraviolet Lithography for the semiconductor manufacturing. As the resolution of the patterns in the semiconductor devices, the corresponding photomask patterns have shrunk during the last decade but the number of the layers has continuously increased. The extension of the EUVL from the wafer-level to mask-level is the enabler of overcoming them. A brief description on the principle of the EUV is given that is followed by the introduction of the developed system, named "UShrinc-Net". Implementation of the UShrinc-Net greatly helps the fine-tuning of the scanner tools after the baseline exposure conditions are set, and it considerably uncovers the possible loss of the best-pattern image quality at the printing-time by monitoring many possible causes of degradation, including fundamental changes in the amplitude of their baseline conditions. The device dimensions in the state-of-art semiconductor manufacturing have been aggressively shrunk over the years of development as the semiconductor industry is the foundation of the modern digital world. Since the early 2010s, the optical/wavelength lithography methods have become the direct replacement of the electron-beam lithography in semiconductor manufacturing and the patterns formed by the optical lithography have shrunk accordingly. This brings severe difficulties as the patterns of the photomask, which is the reduction of the actual device patterns traditionally made by the mask makers, are in the peri-nanometer range. Additionally, the number of device layers that are formed by lithography deteriorates significantly the patterning quality of the scanner tools along with the enhancement of the process window. A possible solution to these problems is to extend the EUV from the wafer to the mask side of the lithography, hence the patterns of the mask and the wafer are subject to the EUV illumination, the same light source. Thereby an important system, "UShrinc-Net" is introduced that encompasses both EUV mask-level and EUV wafer-level lithography, which are actually, up to now, two distinct lithography worlds, and provides the opportunity for the real-time monitoring of the transmission and the occurrence of the defects in the same methodology.

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