Educational Administration: Theory and Practice
2023, 29(4), 5041-5059
ISSN:2148-2403
https://kuey.net/

Research Article

AI-Enhanced Signal Integrity Assessment for High-Frequency Chipsets in Next-Generation Wireless Systems

Goutham Kumar Sheelam*

*IT Data Engineer, Sr. Staff, gouthamkumarsheelam@gmail.com, ORCID ID: 0009-0004-1031-3710

Citation: Goutham Kumar Sheelam (2023), AI-Enhanced Signal Integrity Assessment for High-Frequency Chipsets in Next-Generation Wireless Systems, *Educational Administration: Theory and Practice*, *29*(4), 5041-5059
Doi: 10.53555/kuey.v29i4.9945

ARTICLE INFO

ABSTRACT

Next-generation wireless systems in 6G and beyond foresee increasing interest in chipsets with higher frequencies, including up to WLAN frequencies of 60 GHz and below. Consequently, to maintain signal integrity for these high-frequency chipsets, there are stringent requirements on the PCB layout as well as the antenna-mask fabrication and placement on the PCB. While technological progress has been made on the chip design side and the PCB fabrication side, the signal integrity assessment of the 3D and heterogeneous assembly process is still mostly based on traditional EM simulations, lacking efficiency and intelligence. Instead, a completely new paradigm with AI-enhanced signal integrity assessment is introduced. Benefiting from modern advanced high-performance computing, a 5G chip assembly with ultra-accuracy requirements on signal integrity is studied with a mixed-fidelity approach. Due to its length, the typical hotspots are unseen by exhaustive simulation. Hence, deep learning techniques are employed to accurately identify potential hotspots very fast. An antenna-electrical coupling case study with ultra-lightweight AI architectures shows promising performance on accuracy and speedup.

A comprehensive DQA framework is proposed to assist the AI wireless community in analyzing the DQA problems. Under widely used DQA criteria in the AI model training phase, the proposed framework consists of three tasks to measure the quality of the wireless air-interface data in terms of performance DQA metrics, whereas the effectiveness of the proposed framework is confirmed by validating it on two wireless air-interface data sets. Due to the fundamental limitation in the quality metrics of the synchronous analog data, a task-specific DQA framework is thoroughly benchmarked to fill this gap. With this proposed AI-enabled DQA framework, the DQA of diverse wireless air-interface data can be assessed. Efforts in smoothing the edges of ideal IQ maps and curating additional noise on the existing IQ maps are shown to enhance the robustness of NN models.

Keywords: AI-enhanced design, Signal integrity, High-frequency chipsets, Next-generation wireless, 5G/6G systems, Machine learning, Electromagnetic interference (EMI), Crosstalk analysis, High-speed interconnects, RF performance, Chipset modeling, Time-domain analysis, Frequency-domain analysis, Noise reduction, Deep learning in hardware design, Wireless communication systems, Predictive signal analysis, PCB signal integrity, System-on-Chip (SoC), Design optimization

1. Introduction

Due to the continuous growth of demand for higher-performance & lower-cost user equipment in next-generation wireless communication systems (beyond 4G/5G), the sixth-generation (6G) mobile communication system vision has been initiated through the Development and Promotion of New Services of IMT-2030 and Beyond. Since then, many organizations and research institutes have started to explore 6G air interfaces, service scenarios, business models, and key enablers. AI (Artificial Intelligence) has been regarded as a key enabler for 6G, while the requirement for high-quality data to learn AI models has yet to receive enough attention. Using AI to re-design and enhance the current wireless communication system (including a fundamental re-design of transmitter/receiver, decoding/encoding, waveform, and protocol) is a promising

pathway for 6G. Wireless air-interface data, as a critical operation input for AI-enabled services/functions, are ones collected, transmitted, received, and processed through the air in a wireless way. The dataset impacts the learning performance of an AI model. In addition to the data size, the quality of wireless air-interface data is crucial in determining the performance of AI-enabled wireless communication systems.
Quality assessment of wireless air-interface data can provide insightful guidance for data collection, pre-processing, and model training. However, it is extremely challenging to determine the quality of wireless air-interface data due to its dynamic, complex, and nonlinear properties. Some frameworks currently assess data quality from other fields, such as image, text, and speech data. However, none of them apply to the assessment of wireless air-interface data. This data-quality assessment framework includes three metrics to evaluate the quality of wireless air-interface data: similarity assessment measures the degree to which the new air-interface data is believed to be similar to the old one; diversity assessment measures the degree to which the new air-interface data exhibit a variety; completeness assessment measures how much available air-interface data has been captured. To meet diverse AI service needs, it can be further divided into three submetrics: coverage completeness measures the ability of wireless air-interface data to cover the scope of an application domain; scenario completeness measures the ability of wireless air-interface data to include sufficient different deployment scenarios; and condition completeness measures how well the physical condition is reflected in the collected air-interface data.

2. Background and Motivation

Advances in packaging have increased chip speeds, making early signal integrity (SI) and electromagnetic interference (EMI) analysis critical for optimal performance. Chip design must assess data, clock, and power integrity for “zero fail” operation in excessive speeds with low voltages. Key components in multimedia chips at over 2.6 Gbps per channel in a package ball grid array (PBGA) include bus signal referencing, coupling disturbance from patterned interconnects, package via ESD quality tests, drop tests, thermal cycling, PCB crosstalk with lamination, and ESD effects. Standards for chip impedance control are critical for cabling, connectors, and mounting. A verification flow with analysis tools has improved precision.
An urban environment may have multiple signals and noise cannabis fed to various channels. The receiver may limit performance. This limits the number of channel choices, which beats with adaptive speed. implements an attempt to characterize signal sources, trapping them in a specific sequence. For wireless communication, the PCI bus is the primarily used bus type, usually compliant with PCI 1.0 specifications. A 32-bit PCI bus operates at a 33 MHz bus clock rate and up to 132 MB/s, whereas a 64-bit PCI bus operates at 33 MHz and 264 MB/s. Only PCI 1.0 source codes are available, so additional PCI request acknowledge (REQACK) signal trails slow down system speeds and reliability. A built-in self-test (BIST) that passively monitors PCI transactions has also been developed. Wireless air-interface data are tricky and crucial for AI applications to be deployed. Signal quality degradation may arise from sampling, quantization, storage, defense, and processing. Insights that give clear guidelines for data quality assessment (DQA) of wireless air-interface data and related datasets are broadened. Also, a general DQA framework is provided. Rank and Monte Carlo algorithms and GPR-based hidden variable learning methods for Bayesian inference, probabilistic dynamic models, and Newton and gradient-descent optimizations for training and regression design are suggested.

3. Signal Integrity Fundamentals

Signal integrity captures the characteristics and quality of transmitted voltage waveforms across a physical medium. A signal is a representation of a transmission that varies with respect to time. A voltage signal consists of single or a sequence of voltage pulses superimposed on a DC component . Signal integrity characterizes the signal’s quality through such parameters as slew rate, edge rate, overshoot and ringing, delay and jitter, fundamental and harmonics frequency, frequency spectrum and peak-to-peak and rms voltages. During transmission, the fidelity of the signal is influenced by the electrical properties of the physical medium. Signal integrity analysis focuses on the review of the transmitted waveform such that the transmitted signal captures its defined characteristics by the time it arrives at its expected input.

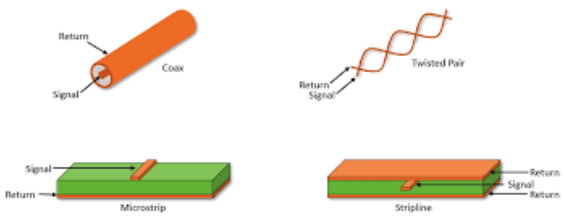

Fig 1 : Signal integrity basics

Signal degradation can occur in many physical characteristics of the signal waveform. The analog nature of continuous signals aids in the visualization of signal integrity problems. Several problems associated with copper interconnects are signal attenuation, ringing and overshoot, delay and skew, and frequency dependent

losses. Transmission line impairments are significant contributors to signal integrity concerns. Such impairments are modelled as Shunt capacitance and series resistance which respectively result in bandwidth and amplitude reduction.

Crosstalk is a common SI problem as it is innate to coupled lines. Lines are coupled capacitively by the shunt capacitance to delay and amplitude degrade coplanar lines, and inductively by leaked coupling from a wide line's lower ground return to upper ground fanned-out lines such that adjacent lines can distort steep transitions. Coupling un-accounts in a single line's different time signals seen at another line, hence temporal degradation once unwound returns at a driver pin.

Power delivery network (PDN) connects a supply voltage to all digital devices. Digital transmission circuits involve multi-voltage domains which rapidly switch their operations from inactive mode to active mode resulting in common SI problems. Tight PDN approximation using fractal geometry displays the rapid supply voltage fluctuations on both high and low frequencies as a result of time varying current-steering amplifiers. Because of the finite inductive inductors and parasitics on the PCB, rapid current spikes drain temporarily through the reference via inducing a voltage drop, hence amplifying a digital signal to distorted levels.

3.1. Definition and Importance

The emergence of high-frequency wireless communication systems is being driven by key social and science/technology trends such as the rapid growth of smartphone users, commercial deployment of 5G networks, and the imminent uptake of next-generation electronic communication systems [2]. These systems present new challenges associated with high-frequency (potentially up to >100 GHz) operation that increases system-on-chip integration and design complexity. In multi-gigahertz chips, signal integrity (SI) assessment is becoming a critical concern, as chipset errors due to losses in off-chip inductors/interconnects or parasitics in active devices cannot be easily mitigated through the conventional use of design rule checking (DRC). A need has emerged for novel automated SI-extraction techniques that are reliable and widely accessible both in terms of the skill-sets and design tools required.

Eqn.1:Time-Domain Reflection (TDR) Coefficient

$$\Gamma(t) = \frac{Z(t) - Z_0}{Z(t) + Z_0}$$

- $\Gamma(t)$: Reflection coefficient over time
- $Z(t)$: Instantaneous impedance at time t
- Z_0: Characteristic impedance of the transmission line

Patch-based and AI-enhanced estimation methods for signal integrity (SI) assessment of high-frequencies have been proposed. The former is an AI-enhanced estimator of useful on-chip SI metrics, utilizing generatively modeling knowledge in spectrum estimation, while the latter is an intelligent tool-chain designed to assist with design exploration and verification in AI-enhanced systems. Conventional SI assessment is performed using brute-force simulation of electromagnetic (EM)-based simulators, requiring extensive expertise and HDL knowledge. This description is unsuitable for design iterations due to the inefficiency of this approach. To bridge the gaps of low-fidelity design-time approximations and high-fidelity verification-level checks, an unsupervised decomposition-based modeling strategy is provided to extract low-complexity and physics-aware SI models through AI-enhanced estimation [1]. These models are very accurate given low complexity and are useful for enhancing signal integrity. The proposed approach is physics-agnostic and widely applicable, therefore allowing anyone who can run commercial design tools to utilize the same technology.

3.2. Common Signal Integrity Issues

In advanced semiconductor processes, where wire widths and spaces are smaller than the design rules suggest, coupling is of even greater concern. These couplings can be averaged over a time duration, but at the high frequencies at which these circuits operate this method of analysis may ignore critical analog information. As these ICs become faster many designers are making the move to multi gigahertz speeds. On a local chip, isolation may be achieved through power distribution techniques and techniques in circuit design. But when a mixed signal chip is placed on a board close to other high speed data chips greater care is required. In such an environment equally important is the chip-package and package-board transitions and the board environment. These multi gigahertz transitions can be modeled as wave propagation in 3D volumetric solvers that include dielectric and metallization defined mathematically through partial differential equations. Once the signal has propagated to the air foundry, modeling is simplified to plane wave filtering and interference. The following sections deal with optimal geometrical constructions over control over the probe waves, and the probe noise sources.

Next generation chips must deliver competitive advantages over currently deployed systems by orders of magnitude in terms of integration and higher frequency operation. Current teardrop simulations have not accounted for the wideband signal propagation and simultaneous optimization of the board environment with the IC layout and package plan must be performed in order to comply with this control over the global noise. It has been shown that detailed coupling analysis needs to be performed at all levels of design from layout to laboratory to estimate comparative on-chip noise levels. Advanced analysis and design tools that truly represent ICs are needed to fabricate system-in-packages for high performance, low power portable applications.The new generation receiver is fiercely competitive, and world leading companies have invested past and future major efforts to design and fabricate advanced CMOS and SiGe BiCMOS devices and chipsets. Short-to-multiple-wavelength and wideband environments, as well as high demand assembly technologies have created a large business area. Communications are rapidly growing from narrowband to short-range multi-gigahertz systems. Roll back of the communication technology curve provides the best opportunity for strong contributions. Due to the microwave to millimeter-wave-device technology gaps, one-time collaborators of lateral CMOS technology have teamed together to employ high-volume chip-carrier assembly techniques to complete and package RF front ends by passive-filtering disintegration of the chipsets.

4. High-Frequency Chipset Design Challenges

Ultra-High Frequency (UHF) operation at 60 GHz has several advantages for next-generation wireless systems, including ultra-fast data exchange, networked devices replacing physical connections, and highly integrated/miniaturized packaging. However, wireless systems operating at such high frequencies face several chipset design challenges, particularly with regard to the Passive Integrity Assessment (PIA) of sub-millimeter-wave Passive Devices (PDs) . Without sufficient testing, design and fabrication processes induce variations in PD physical and electrical parameters, affecting QoS and coverage provided by transmission media. Potential method extensions to millimeter-wave ranges are examined in terms of design challenges.

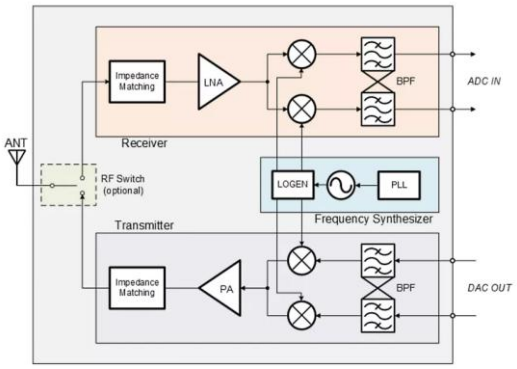

Fig 2 : Radio Frequency Integrated Circuit (RFIC)

Over the last few years, the networking of electronic devices has gained immense popularity. High data exchange performance is required between these devices, making electromagnetic transmission media a preferred solution. In addition to ensuring the coverage area and quality of service (QoS) provided by the transmission media, the design and verification of wireless data transfer systems face significant challenges. Wireless data transfer is simpler and involves fewer hardware components compared to wired data exchange systems. Wireless systems only need an RF frontend and a transceiver chipset to transfer data wirelessly. However, traditional Integrated Circuit (IC) design and verification challenges are intensified in the RF domain because of the operation frequency. Sub-millimeter-wave RF Simultaneous RFID Reader/Writer chipsets operating at 60GHz are currently being developed, capable of integrating the mixed-signal RF and digital building blocks of the transceiver chains on a single RF System-on-Chip (SoC) die. However, the design of high-frequency PDs in Active and Passive Integrated Circuits (ICs) is not trivial and involves major challenges. This is particularly true with respect to the PIA of sub-millimeter-wave PDs because the fabrication temperature, environmental conditions, or aging effects induce deviations in PD topologies and tech-model parameters, affecting the physical and electrical verification of the PDs. To maintain high product yield and QoS for high-frequency transceiver chipsets, suitable signal integrity assessment methods are urgently required.

4.1. Material Properties

Accurate knowledge of material properties such as dielectric constant and loss tangent is of paramount importance in the analysis and evaluation of the signal integrity performance of high-frequency PCB boards. Several techniques have been developed to characterize these properties at lower frequencies and therefore, extensively used in the PCB design community. Sadly, these techniques fail to meet the demands in the high-

frequency domain. As a result, characterization of the loss in PCBs becomes an arduous task as the frequency of operation increases beyond 5GHz. A hugely different challenge is the characterization of the loss in PCB substrates, which is an order of magnitude more difficult than the microstrip line loss characterization. Chip/Substrate stack-ups are complex and involve multiple layered structures of different materials of different physical properties. Likewise, the measurement is further complicated due to measurement de-embedding and packaging to board interconnect de-embedding. Hence a comprehensive model for the entire compatibility of device to PCB stack-up is developed. On the other hand, as the size of the channel increases with technology scaling and the number of channels integrated into a chip continues to grow, signal integrity has become not only crucial but also complex with multiple factors playing a role. As interconnect dominates the delay with increase in frequency, interconnect modeling has also taken on a renewed importance. Therefore a kernel based efficient approach is proposed for PCB/Package level interconnect modeling. The recent advancement in packaging technology has led to die with hundreds of I/Os which require complex higher order interconnect networks. Next generation packaging would integrate Die from different vendors on different process technologies. RF I/Os from Silicon-Germanium would connect to a ultrafine pitch PCB of capacity as small as 300 micron at high mmW frequencies. Therefore robust multi-chip packages are developed as an extension of 3D packaging over the last few decades for heterogeneous integration.

4.2. Thermal Management

Among several thermal management methods suggested, the topside thermal management method is selected as a relatively good solution to solve overheating issues in SoC and multi-chip modules. A topside thermal management solution can be easily attached on top of any conventional device packages without any redesign of the packages, resulting in fast deployment and low cost. Since the specified topside thermal management solution is not ready at the initial system design stage, a few approaches to evaluate the potential thermal management solutions quickly based on existing infrared thermal data are developed.

One proposed method is a thermal network-based topside thermal management device evaluation method. While measurement data are used as boundary conditions of chip losses, steady-state temperature maps are obtained as an output. As one of the ongoing works, a simple but necessary sensitivity analysis to characterize the fast and slow modes of a pixel and guidance to avoid potential quick mode saturation are provided. This method is capable of assessing commercially available topside thermal solutions on the corresponding package for a fast and practical thermal design.

Another proposed method is a lumped model-based approach to evaluate the severity of heatsink or die-attach level design issues over other package level design issues. This provides a straightforward interpretation of the thermal performance in terms of lumped thermal nodes, significantly speeding up the evaluation process at an earlier design stage. This method was used to explain why some products overheated in the post-layout simulation stage.

In one of the ongoing works, a few modifications are made to the transients path analysis thermal projection method, which can be used to detect uncharacterized and unmonitored hotspots on chips or packages. Based on spectral analysis, the method is extended to other frequency band analyses to better understand complex cases. A radiation-based relationship between hot spots and temperature readings is established as a speed-up way to calculate temperatures from the hotspots. As an ongoing work, a regularization-based method robust to noise is currently being developed.

4.3. Electromagnetic Interference

Next-generation wireless systems such as 5G, Internet of Things (IoT), low Earth orbit satellite communication systems, and autonomous vehicles require the implementation of high-frequency RF front-end chipsets. Complex System on Chips (SoCs) with data rates exceeding 1.5 Gbps and transmission frequencies exceeding 6 GHz increase the integration of multi-port signal lines within a tiny space. Thus, ensuring the integrity of LPWA (LoRa, Sigfox) and high-speed multi-gigabit CMOS wired serial links is regarded as one of the greatest challenges for the designers of next-generation high-performance wire line and wireless systems [4].

Consequently, routing essential short differential signal lines within the critical active areas covered with RF lineup is significantly challenging. Typically, 3D layout is utilized to comply with complicated design requirements such as the system package design rules and the electromagnetic compatibility of chipsets. Advanced algorithms, such as AI or an electrical circuit model, are actively adopted to analyze the high-speed signal integrity issues without full-wave solution. The complicated layout rules and RF front-end topologies greatly increase the simulation time of signal integrity analysis. Current alternatives for signal integrity simulations still require at least half an hour per circuit in an idle condition. Therefore, an efficient solution is mandated to tackle the time-consuming signal integrity workflow for a design loop-based platform considering various designs. This research actively regards the complex 3D EM package design as a masked black-box function without any prior knowledge of layout rules and circuit features. It can quickly estimate the performance of complex designs in less than one minute without seeking all parameters based on a two-level synthesis design including Random Forest Classifier and Gradient Boosted Tree.

Next, the AI-Enhanced Signal integrity assessment is actively investigated to assess the integrity of high-speed chipsets based on Recurrent Neural Networks and attention mechanism, which is regarded as another black-

box function without explicit timing charts, circuit models, or simulation rules. Embracing the outer black-box functionality brings additional benefits concerning various designs and simulation tools. Closing the signal integrity items and related circuit models enables the ability of year-round optimization and transcending design teams effortlessly.

The ultimate experimentation validates the feasibility of above research. It is a synergistic design environment that can automatically evaluate, enhance and re-design the signal integrity of high-speed digital circuits, indicating better signal integrity of performances with optimization and outperforming delays with even huge electromagnetic layouts and complex signal integrity analysis.

5. AI Techniques in Signal Integrity Assessment

Emerging AI technologies, some of which have been brought to high-frequency signal integrity characterization and realization problems, are already at the forefront of research. The rationale for harnessing machine learning algorithms for critical and noncritical tasks such as performance evaluation, simulation, and optimization of high-frequency circuits and interconnects, as opposed to conventional techniques, is laid out. An advanced AI-enhanced platform is described in detail. Several practical case studies, including joint disparate AI techniques for performance evaluation and optimization of a high-speed gigahertz flip-flop chip, illustrate the solutions' capability, accuracy, and efficiency [5].

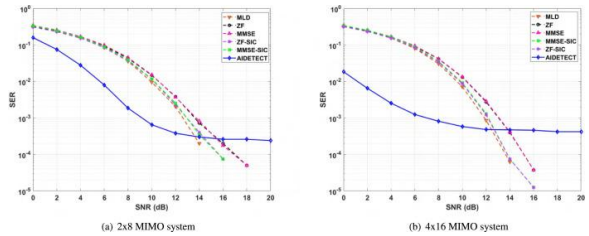

Fig : Artificial intelligence-enhanced signal detection technique for beyond fifth generation networks

With the rapid growth in data rate required for communication and computer systems, GHz or even THz chipsets have been pursued to enhance throughput. However, signal integrity issues such as inter-symbol interference and increased crosstalk noise have become more pronounced with technology scaling and are more challenging to assess. To ensure a successful chip implementation, computationally intensive simulations need to be carried out for 1–10 billion input patterns post-layout. Advanced AI techniques, including self-supervised and semi-supervised methods, have been proposed for faster assessment on the unmodified layout with good accuracy. In addition to this, a chip layout modification is also investigated to suppress crosstalk noise. In this regard, the proposed variational graph neural network is able to locate gates on the layout by coarse-to-fine adjustment with just 50 candidates tested for the top ten gates.

Unlike conventional endorsements such as performance assurance via worst-case conditions and predictions through minimum resolution and protection tests that generate samples at a rate of 1/100,000 times of operational patterns, machine learning-based approaches are able to generate performance assessment models effectively and efficiently. Adequate training and loading can help achieve simulation speeds as high as 10 million patterns per second with accuracy within 3% of the compact lookup table models used in production. The prospect of wide deployment in production is promising. As a first step, focus is placed on helping designers by providing golden performance and fault models as bronze assets.

5.1. Machine Learning Approaches

Machine Learning (ML) is ushering in a paradigm shift in numerous fields, paving the way for new frontiers. Modern ML techniques, such as Neural Networks and Reinforcement Learning, have been deployed in real-world applications such as automated speech recognition, facial recognition systems, and AI-enabled games. The rapid advancements in Machine Learning (ML) have enabled a new generation of AI-enhanced wireless communications, including channel modeling, channel estimation, transceiver design, array beamforming, and mobile communication system design.

Despite the great strides that have been made in ML, there remain several challenges ahead. In the field of radio propagation, physical modeling approaches are currently relied on to model the wireless channel. However, physical modeling efforts are mostly based on lowest-level physical principles, which are often cumbersome, challenging, and time-consuming, prohibiting routine use during the design and optimization phase of wireless systems. While traditional model-free ML techniques have been developed for radio propagation, they are often criticized as a black-box approach, and runtime performance can be poor, in the order of seconds or even longer. A combination of physical modeling and AI techniques thus can potentially lead to a model-assisted AI approach, as a means to turbocharge MC-based scenarios with difficult environmental conditions.

The placement and nature of AI in physical modeling is a new and less explored area. Meanwhile, there is a growing interest in harnessing the power of AI in many upcoming applications, including but not limited to radio propagation, which exhibits characteristics fundamentally different from indoor scenarios: Anisotropic scattering motivated by many (as opposed to few) scatterers; rich temporal variations, ranging from milliseconds to seconds; and inconsistent scenarios depending on the user mobility. These challenges warrant usage of new AI techniques perhaps different from what are mainstream in the indoor or more traditional setups.

Eqn.2:Signal-to-Noise Ratio (SNR)

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}}$$

- P_{signal}: Power of the desired signal
- P_{noise}: Power of the noise affecting the signal

5.2. Neural Networks for Signal Analysis

The performance evaluation of high-frequency electronic devices is usually analysed and optimized using numerical simulation packages that are time consuming. Hence, a fast model is proposed to predict easy-to-use signal integrity (SI) performance indicators for the designers. For the sake of obtaining better predictive performance with larger neural networks, the challenging sampling designs of high-dimensional problems are tamed. First, a projection-based dimension-reduction strategy is developed to blurt the sampling points that in each dimension lie on well-spaced knots of a notched spline basis. The time-consuming SI indicators are in situ and iteratively evaluated on the sampling points. Subsequently, a cascading sequential learning method that complacently blends the inverse distance weighting interpolation and backpropagation neural network (BP-NN) approaches is proposed to achieve the predictive model. Final efforts to numerically illustrate the predictive capacity of the constructed models on the coupling effect of high-speed digital chips such as a complementary metal oxide semiconductor (CMOS)-based 28 Gbps unidirectional driver, are expounded. Machine Learning (ML) methods have been proven to accelerate the prediction of various engineering problems by candidate-driven surrogate modelling. In recent years, ML methods have been applied to the simulation and on-chip assessment of signal integrity (SI) performance in wide applications [6]. ANN indicates that imitating the internal structure of the brain neurons, it can process the information about the external environment in a way similar to the human brain and obtain the relevant knowledge. This knowledge is stored in the form of weights. Therefore, ANN can get acquainted with things through an observation process comparable to human memory. ANNs are capable of approximate nonlinear mapping of data based on their unique topological structure. For the design of microsystems, one of the important indicators to evaluate the signal integrity (SI) of the microsystem is the prediction of the eye diagram of a high-speed interconnection structure. The eye diagram is mainly described by eye height and eye width. Then numerous researchers have focused on the prediction of these two parameters. The chip package is one of the essential aspects of microsystem design. The package inductance affects the speed and integrity of data signals through high-speed interconnects, so it must be considered in microsystem design. High-speed interconnection structure in the package is widely used for signal transmission and power distribution. Applications of neural networks to predict the eye diagram of an interconnection structure, composed of a chip surface mount package and a high-speed printed circuit board (PCB) trace.

5.3. Data-Driven Modeling

The interconnect path on the PCB, designed on a high-frequency chip package, is the most vital part in high-frequency circuit simulation, and it is critical to extract dense, accurate, compact, and repeatable data-driven model parameters of the interconnects for the above chip package layout. This path will determine the loss in the time domain and the bandwidth of the circuits and is impossible to extract on the high-frequency level using circuit simulators due to the limitation of CKTS and RTT. This requires building data-driven models using extracted fully distributed SPICE nets and optimizing the SPICE nets, then deriving the model parameters used in the circuit simulators. CAD tools, including Q3D for PCB extraction and QNExS for the circuit simulator, are the tools first used to extract these model parameters. If one wants performance beyond 25 GHz and cannot bear high licensing costs, there is no high-frequency model extraction tool available, opening the door for innovation. Driven by the demand for a data-driven model under 60 GHz, a procedure to extract the densely parameterized RLCG Model C is presented. After the 3D data has been collected, the model parameters are built up by defining an extraction strategy. A set of numerical optimization steps are then implemented to fit spectral behavior, matching the 3D data and the L format, which approximates the energy properties and algorithmic affordability. These Model C parameters are then passed into the AFsolver Parallel Growth Process, resulting in a successfully constructed and validated D-language model. Finally, the parameters are inserted into QNExS V\(3 imes3\) PML, yielding dedicated spectral results which are

match the 2D C version, and successful construction of the 3D D-model for simulation under WHz frequency is completed. Full behavior modeling affects the layout of the next-generation chip in the data center and saving silicon area on the high-frequency chip. This research will focus on a high-frequency smart decision AI scheme used in high-density data centers in the future [8].

6. Integration of AI in Wireless Systems

The rapid advancements of artificial intelligent (AI) provide an opportunity to redefine wireless systems from a simplicity perspective. Different from the classical mathematics-based design methodologies that rely on fully understanding wireless systems, data-driven designs aim to exploit big data generated by wireless networks to derive optimal solutions. AI enables a new knowledge discovery paradigm, which vies with human-designed approaches in many areas, such as reasoning, gaming, and decision making. Thanks to the recent breakthrough of AI technologies, especially deep neural networks (DNNs), AI-enabled approaches are explored in various for next-generation wireless systems .

AI find ways to be integrated into wireless communications, and the challenges facing AI-enabled communication systems are highlighted. Three types of novel performance-aware AI technologies for next-generation wireless systems that rigorously interleave data collection, AI-based design, and performance analysis are presented. Integration of AI and various middlewares—including simulation platform, cloud, and emulators, as well as edge computing—is also discussed. AI, through enabling innovative data-driven analyses, designs, and implementations of communication systems, can spur revolutionary advances in key performance metrics. However, it is still in its infancy, and many research efforts are warranted to unleash its full impact during the development of next-generation wireless systems

The synergy between the fields of wireless communication and AI opens a new software-defined powerful paradigm for next-generation wireless systems. Compared to the conventional mathematics-based approaches that struggle to keep pace with the rapid increase of wireless data scaling and bandwidth expansion, AI-enabled performance-aware DNN infrastructures can effortlessly handle and process large-scale data with the advances of both cloud and terminal-edge computing resources. By getting rid of the tortuous mathematics modeling of conventional approaches, AI-enabled systems are more flexible in searching for optimal solutions in a plethora of data, and robust to varying wireless environment and network changes. Rigorous performance evaluation is essential for both AI-enabled communication systems and performance metrics, while it is still an unexplored area in the existing literature.

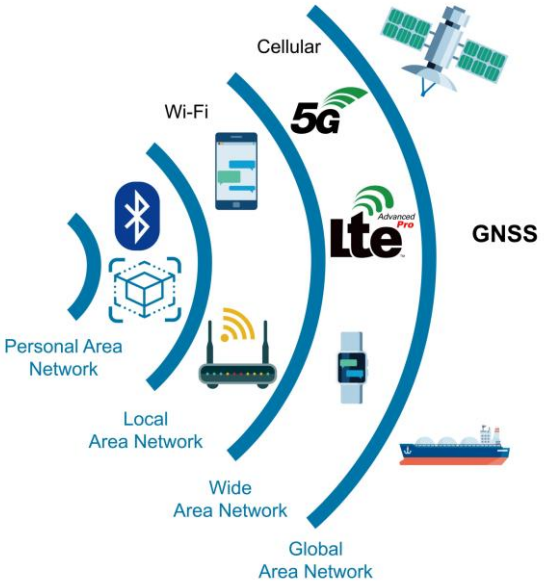

Fig 3 : Wireless Networks

6.1. AI-Driven Design Tools

While many AI tools may be employed to assist the design process steps, design methodologies are of utmost importance to integrate multiple tools into a unified design flow, thus maximizing the efficiency of the AI tools as well as the quality of the design outcomes. The examination of modeling techniques was dedicated to new circuit challenges such as aging, thermal effects, cross-talk, etc., most of which can be learned from AI/ML models but beyond traditional EDA-based models. Moreover, it's crucial to flag out the potential risks in advanced silicon nodes that cannot be directly simulated by the commercial EDA tools, as a predictive model. Once the risk is spotted, it can be discussed with alternative layouts, technology changes, or matching circuitry.

Therefore, there will be a new set of design/analysis tools which are AI/ML-enabled and EDA-connected that bridge the gap.
This section delves into two AI-driven design tools that could be indispensable in signal integrity assessment: 1) a geometry-type design space generator, which can leverage the state-of-the-art DNN models and topology-based generative design; 2) a model structure generator to support the continuous-time signal integrity model generation to build a wideband signal integrity analysis tool for the generated layout.
The signal integrity analysis of high-speed chipsets, which require a proper incorporation of the dielectric layer and interconnections' combination of material and metal in both circuit and physical layout for realizing targeted signal integrity figures of merit, is a data-confined task, especially in GHz and THz frequencies. Traditional design space exploration tools cannot manage high-dimensional design variable spaces due to the exponential scalability. Unstructured and unconsolidated machine-learned layouts may lead to low-quality designs. Conventionally structured graphs and topology-preserving generative design can now work with the academic-level physical simulators to dynamically and efficiently generate high-quality circuit-and-physical layouts, with no major sacrifice on quality.

6.2. Real-Time Monitoring Systems

Remote RF monitoring is necessary for Old and new applications considering the growth of ISM bands and the popularity of unlicensed services. It is well known that remote estimation of the performance of RF devices can be defined. Knowing some pertinent parameters like temperature, component sizing, and others, it is also known when the signal distortion is unacceptable and must be avoided or corrected. Application of this knowledge results in the requirement of new monitoring and test functions to be integrated into all RF devices. This makes the subject highly achievable from the RF perspective. Indeed the quest problem is: How to perform the monitoring task in such a way that it becomes feasible to be integrated on the chip?
It is well known that any RF receiver contains stages for RF frequency down conversion and signal amplitudes reduction. These stages being designed using non-linear components and active circuits introduce distortion to the signal. Monitoring the digital output signal can fail because RF devices intended to work in several RF channels. Missed spikes or anything out of taken converted bits would necessitate changing the whole chip. Since the latter are getting smaller, complex, and sensitive to the electromagnetic environment, old monitoring paradigms based on signal injection are less satisfactory.
Passive monitoring method takes the advantage of sinusoidal self-injection. It inherits the advantages of low complexity, applicability to RF chipsets, and compatibility with high Q-factor filters. Significant focus is put on complex digital systems such as "emulation" of analog devices, analog-to-digital converter (ADC) outputs. Combining with passive RF self-injection schemes, monitoring analog systems' responses with channels unavailability becomes feasible, which is achieved by minimizing performance impact of digital self-injection on processing bandwidth. Some RF performance monitoring methods based on a weak self-injection approach preserve the capabilities of the receiving systems while allowing for undemanding post-processing considerations, applicable to monitor various RF impairments on the performance of different receivers embracing various transceiver architectures .

7. Case Studies

Signals at high frequencies are impacted by physical effects where the scales are close to the wave scale. Path loss and attenuation rely on the atmospheric and physical materials. Chip packages are subject to the PCB's effects, including distortion due to both inductive and capacitive load impacts. Further, multiple antennas for massive MIMO operation are typically connected to a chip through wide bus lines 150- 600 mm long and 0.5 mm wide, which also interacts with the chip and package lumped components. The architecture employed may or may not rely on Digital Pre-Distortion (DPD) interpolation or equalization. To maintain performance, systems must be designed with consideration for these effects. The design process has close connections to modelling and testing as physical effects are studied laterally. How to simulate and model structures that require knowledge of the handling of differential information is but one avenue of research. Building parsimonious models for the entire 3D chip-bus-Package-Channel must use geometric and model abstractions, which is very challenging. Understanding inputs to unified simulation and parametric testing are impeded through lengthy construction times and lack of tools that damage, non-classical, down-sampling, or mixed-mode signal domains at chip board interface. Of great concern is the requirements of new systems in terms of its available geometric and material information.
Sufficiency involves modelling the shapes of the package, deformities or bonding materials, coating conductors, assumed distribution of isotropy, or statistical agglomerative arrangement of materials. The power of p, S-parameter data QC considers only staple circuit models reference idealities, similar models in DPA's tools, and even physical modeling numeric solvers [1]. In DPD, it is sufficient that EVM, PSR or spectral measures beyond 1 GHz are baseline tested using fragment, not complete, modelling and testing information, as circuit paths or large systems are often discarded. To help this complexity and capture modelling where it is used as part of package design or for modelling non-focused (array/multiple antenna applications), End-to-End (E2E) Assessment is introduced to also understand efficiency. E2E assessment is general, applicable to any high-frequency-chip exposed to arbitrary ingredient distortion. The automatic synthesis of a designated E2E model

and transient characteristics is done. Radar and EVM measurements are used to assess and correct model and test mismatch for a 1 mm GaN power amplifier IC. E2E includes a generic partial spectral QC method for linear processing systems based on a state duality and derivative gauge domain modelling (E2E-QC), an automatic model synthesis and nonMH testing density construction and Drive-By-Detection (DBD) method (QC-E2E). Further understanding of prediction and causal path and distortion separation robustness is included.

7.1. Case Study 1: AI in 5G Chipsets

A case study on 5G chipsets is presented in this section, discussing their information flow, AI-enabled features, data collection, and validation methodology. The exemplary use case analyzes the advantages brought by AI integration of baseband processing relating to enhancement of signal chain, detection and decoding.

5G is the fifth generation of mobile wireless systems succeeding LTE. It is primarily driven by the pursuit of higher data rate, lower latency, and more devices. A new air interface, namely NR, is used in 5G. In addition to order-of-magnitude increase in complexity, many new technologies are introduced in the NR air interface to support its vision. These include: ultra-dense deployment, massive antenna systems and waveforms.

To cope with the more aggressive transceiver designs of 5G chipsets, new RFIC architecture becomes the foundation of the 5G signal chain. Architecturally, the 5G RFIC consists of an array of sub-chips with several digital blocks and a common analog backend. This baseband architecture tightly couples RFIC and BBIC for optimal performance.

The chipsets for 5G systems in the Sub-35 GHz frequency bands have been developed from concept to production, covering: customized RF systems-on-chip with ultra-low power, high-order wide-band thermal self-calibration and phase interpolator clock alignment, as well as high-dynamic range highly-integrated power detection and digital calibration. The 5G analog baseband was developed with improved DSP and new high-dynamic range high-performance ADC/DACs.

The chipsets have been validated against the latest standards. The post-silicon validation requires methodical and elaborate procedures to ensure the end-to-end performance, which may involve: functional verification on chip, board, and system; Power-on tests of all blocks; Verification of power characteristics; Baseband subsystem validation, etc. If any deviation from the specification is found, the corresponding fix should be implemented within a minimal wait time. Automated, high-performance, high-throughput, hardware-in-the-loop validation environment has been built for on-wafer rapid validation of 5G RFICs and systems, which has been successfully applied to the 5G mmWave RFIC for both performance and production tests.

The introduction of AI into mobile communication opens unprecedented opportunities from the perspective of different layers. Although most relevant research focuses on AI-enhanced data or signal processing schemes, an essential requirement for deploying AI algorithms is to ensure the input data quality.

7.2. Case Study 2: Impact on Signal Quality

As a second case study, this section discusses assessment augmentation. For the purposes of analysis, some high-frequency chipsets are selected from an attractively available tool. Their robustness against crosstalk-induced signal-integrity degradation is assessed with statistical inputs for their parametric, crosstalk, and operating voltage variations. Shown are the calibration output measures, eye-pattern histogram, and selected samples of the eye-pattern traces, respectively. It is notable that the post-layout signal-integrity assessment of this high-frequency design is severely challenged due to strong signal-integrity degradations caused by crosstalk in a few layers.

Moreover, it appears that the previous half a century of innovation and design efforts for tightening timing-skew of multi-layers only results in moderate enhancement on the performance of the designed high-frequency chipsets. Seen are the output measures of signal-integrity degradation due to crosstalk on some selected output pins (or traces), in the post-layout scenario of the initial refinement signoff. The behavioral eye-pattern trace for the core design (with crosstalk inputs disabled or all eigenvalues set to zero) is shown on the top row, which is free from signal-integrity impairment.

This, however, fails to maintain its quality and deteriorates rapidly upon the introduction of crosstalk, and an array of unwanted glitches appears. It is notable that in the testbench at least one of the input pins is excited with a periodic input stimulus, while all outputs (except for one pin) are defaulted to a logic-up level. Although some eye-pattern traces at minor crosstalk, crosstalk-to-crosstalk delay mismatch (within a couple of unit intervals), and input/redundant pin excitation (due to internal encoding structure) are left unaffected at the output, the amplitude degradations are severe elsewhere. Input pin activity is an important condition on robust output signal quality, thus, the corresponding eye-pattern traces are not addressed here.

8. Experimental Setup

Figure 1 illustrates the basic components of the proposed AI-based signal integrity assessment framework, which collects data from the chipset on the testable board (T/B) channel in the product's environment. The two most common integration levels of high-frequency chipsets-in-system-on-chip (SoC) form factors are surface-mount device and chip-on-board (SMD) with traditional silicon die packages. After assembly, the embedding board is probed. Broadly, the performance comparisons include delays (skew), mask violations (Jitter), integrated test, and on-chip/board diagnostics.

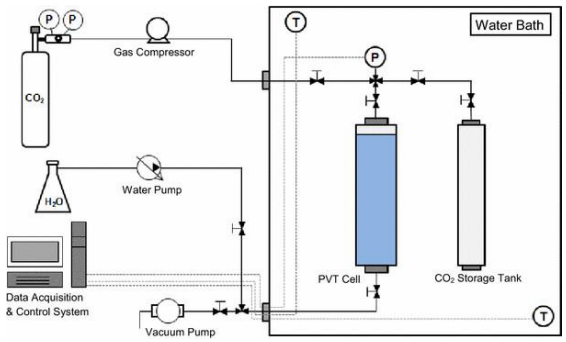

Fig 4 : diagram of experimental setup

Physical Layer Compliance testing of generation 1 wireless standards is attainable with solely hardware functionality test requests. A common paradigm is to generate a frequency-sweep signal to evaluate a DUT response score. Figure 2 elucidates three classes of test assessment: Class-I uses a computing resource to produce a component score from a live output such as an eye diagram. Class-II applications largely work based on pre-computed tolerances on assessable waveforms. Class-III assessments pose a probe position and test waveforms, and raise a numeric response.

Significant additional challenges arise in both the design and test/diagnostic of next-gen ultra-wideband wireless chipsets. Besides scalability to sub THz, this generation fundamentally differs in pair-wise focused digitization on chipsets and multi-standard compatible but incompatible high-speed interconnects switching topologies. Many timescale signals must be traceable while hope for same-time integration at 100x pin-counts. Domains onboard probe array and channel-hit unit assessments must be addressable.

Proper physical bounds on propagation times and equipment latencies from assembly to chipsets, and tracer-board locations in-between must impose signal distance range mappings. Setups of next-gen test equipment include the entire test context: configurable setups, a fixture or socket structure, and an architecture that interconnects both with the D.U.T input-output and the SUT control interface.

8.1. Testbed Configuration

Figure 8.1 shows the testbed configuration used for the OTFS signal generation and processing. The inputs to the testbed were 8 × 8 matrices of ULA antenna indices at tx and rx, respectively. For each tx and rx, the codebook was designed to sweep the beam directions across the antennas using the azimuth angles with n ∈ {0, . . . , 63} and elevation angles with m ∈ {0, . . . , 1}. The tunable phase shift generator, which generates different phase shifts according to the index generated by testing different indices for each antenna, may be implemented by micro-electromechanical systems, or RF-photonic integrated technologies. To obtain the expected output covariances after sampling, these devices were integrated with the microscope objective lenses and multi-data acquisition 8-channel passive playing circuits, and connected with a PC load, and programs to collect the multi-channel sampled outputs.

This testbed was tested by simulating the wideband OTFS generation with beams at baseband using the method in Sec 4. The frequency was fixed to f0 = 9.8677 GHz. The number of taps, k, was taken to be 2, the transmit filter bandwidth, Btx, and the receive filter bandwidth, Brx, were set at 1 Sud, and the tap delays were θ1 = 0 and θ2 = 5. The time-horizon of the training signal was set to T = 24s. The tx/beam covariance, QAvg, was assumed to be a constant matrix. The receive covariance, Rw/o n, was driven by stationary narrowband processes wt and noise n(t). A set of receive covariance outputs, Rw/o improved_SNR, were considered, with noise-free outputs, Rw/o n = Rw/o improved_SNR = Rq, with the white output covariance, Rw/o stationary, and colored outputs, Rw/o nonstationary, experiencing a group of time varying low-rank process. The GN iteration was used to obtain the parameters of the grasping windows. The corresponding engulfing window, g = the expand R0 * R,* R0 = R yearly manual.

8.2. Measurement Techniques

The accuracy of interconnect-to-chip signal integrity assessment depends heavily on whether or not the test access is available at the interconnect-meets-chip interface. Nowadays, most of the test access methodologies proposed for system-on-chip chipsets rely on embedded pads that are compatible with the boundary-scan standard. In an environment where the chips are stacked into multi-chip modules or packages, this test access is often severely limited. For example, in many flip-chip bonding processes for ball-grid-array packages, the only interconnect access visible is a series of solder bumps connected to the chip's pads, and these bumps are embedded in an epoxy under-fill. As a result, during the BIST operation, the chips in the package are isolated from the outside world, and detecting interconnect-related fault modes is impossible. Nonetheless, this test environment allows a reduced bit-width fault detection hardware implementation feasible. Accordingly, this chapter will also highlight the emerging field of comparable gate-level fault diagnosis solutions, which can dramatically shorten the guard-band time considerably.

Eqn.3:AI-Predicted Signal Integrity Score (Regression Model)

$$\hat{y} = \beta_0 + \sum_{i=1}^{n} \beta_i x_i + \epsilon$$

- $\hat{y}$: Predicted signal integrity score (e.g., eye height, jitter tolerance)
- x_i: Input features (e.g., trace length, dielectric constant, via count)
- β_i: Learned coefficients from AI model
- ϵ: Model error/residual

The trend for measuring the power integrity metrics presently begins from the SoC package and goes to the chip level. But, what aspects of power integrity data need to be measured at the chip package interface? The worst-case and the best-case power/ground voltage simulation models are used to diagnose the expected worst-case power integrity metrics and evaluate worst-case margins, which in turn should guide power integrity measurements during the DFT for production. While considering a real-time measurement, index changes are going to happen at an operational mode in the chip. Therefore, it is also essential to accumulate the measured results in respective index bins. The power/ground noise during index changes can easily be lost if the noise spikes are short. So, the operation mode delays should be set large enough to ensure capturing worse power/ground noise. Prior to mass production, characterizing an SoC flip-chip package is often the process of running functional tests on the SoC at-speed and chip-level, thereby testing the ball grid array solder bumps attached to a PCB. In production, the same packaged part will typically undergo lower-frequency and lower-voltage tests that will stress and precondition the connections for a short time prior to running another set of tests.

9. Results and Discussion

Next-generation wireless standards such as Wi-Fi 7, 5G, and 6G are predicted to employ vigorous modulation formats for both proprietary and cooperative standards to improve spectral efficiency and thus increased coverage with higher data rates. Such increased requisites in wireless systems demand closer integration of the Analog RF and Digital Baseband for signal integrity evaluation of the chipset. However, with increased data rates, the key signal integrity assessment numbers like jitter, Eye Height, Eye Width, Eye Opening, duty cycle distortion, etc need Computation Time efficient approximations from the traditional exhaustive and CPU hungry methods. It is envisaged that, with Multi-Simulated & Artificial Intelligence prediction based data samples of these key signal integrity metrics from swiftly simulated configurations; the massive signal integrity data assortment will be successfully designed for next-gen wireless chipsets of 8X8 up to 40 Gbps. Lastly, it provides the framework for numerous applications in IC SLA, Circuit Design Co-simulation closure, etc.
In this paper a 'time-domain' Data Quality Assessment framework is proposed for various AI-enabled 5G/6G chip-sets to assess the quality of the wireless air-interface data so that it can be used to train AI/ML models. Here a versatile channel modelling framework is suitably utilized to co-simulate 5G/6G core devices along with S-parameter-based RF Front-end chipsets and a DQA module is designed to evaluate the quality of the wireless air-interface data. DQA algorithms in the frequency-domain are readily available but there is a rising need for time-domain DQA algorithms as conventional measurement-based fidelity verification methods tend to work only in the frequency-domain. Several necessary metrics are introduced to quantify the fidelity of data at Transmitter, Channel, and Receiver ends. Each of these metrics is designed to be efficient in terms of computation time and computational resource usage, making them suitable for real-time performance monitoring and quality control of AI-enabled wireless communications.
Lastly, state-of-the-art applications such as similarity and diversity assessment, sampling and interpolation, data-fidelity verification, data sanitization, and data augmentation are demonstrated in the context of CSI data. Results reveal the versatility of the proposed framework in terms of the types and complexities of AI data that can be assessed as well as maximally exploiting the quality of wireless air-interface data, thus enabling the optimal performance of AI-enabled wireless communications.

9.1. Performance Metrics

The assorted kinds of digital distribution layout analysis and verification techniques can be classified with respect to the following PPA change metrics: Digital Layout Efficiency Checks, Digital Layout Noise Check, Digital Layout Power Demands Check and Payout-Sign Off Checks. The first one actually compares distributions for violations of switching activity, buffer count, layout area and interconnect duration metrics. Post-Place & Route Extraction and post-Place & Route Simulation are common practices in the industry for evaluating noise output of the digital design layout, in order to flag possible digital block to mixed signal interface concerns. The DPF DRC are stepwise validated, from Golden Design to Diamond Design and Diamond DRC.
Parameter, Modal & Mixed-Mode Verification are the check steps focused on design reliability issues. For designs that employ Header configuration for Test-bus designs for 3D integration and Embedded Memory

build, a combination of state-of-the-art DFT techniques enhanced with Wrapper BIST and Scan Test technique should be used and designed as early as possible so they can be included in netlist and standard cell library, enabling plug-in co-simulation with EDA tools.
Payout-Sign Off Checks are co-simulation based verification flows of DA as designed data based with real Life Load Condition Timing Check flows and DRC to Cast and Pack. Report level and cross hierarchy verification are widely used to edition stories or generation media.

9.2. Analysis of Findings

A potential candidate of interest for the next-generation wireless systems is an AI-Enhanced Signal integrity assessment for high-frequency chipsets. The current work aims to develop a compact, fast, and accurate platform through the 3AI approach and AI-SHINES suite and demonstrate its usage with a low-power wide-area network chipset. The platform highlights the need for similar works to push the state-of-art of AI-enhanced signal integrity assessment tools further in terms of accuracy, scope, and speed. The ongoing and prospective developments are also elaborated on, indicating current future work at both software and hardware levels.
To speed up and automate the signal integrity assessment of next-generation wireless chipsets using AI-enhanced functions, a collaborating hardware/software approach is presented. This comprises a platform-level generic hardware described with a modular architecture concerning cost vs performance and integrable with beneficial surrogate modeling techniques in the context of AI-enhanced p–c and a software suite of custom-built AI-enhanced algorithmic functions for large-signal distortion monitoring at various simulation levels. A flexible family of high-level abstractions to link about vendor-agnostic C++-based library addressing signals and system through commonly used tool kits in this field is also introduced. Reducing the signal integrity task development and tuning time is another role of this generational choice in conjunction with hardware-accelerated large-scale random walk sampling input generation in the fastest hardware vendor-supported functional language. Each platform level of AI-enhanced signal integrity assessment for next-generation wireless chipsets is illustrated with a custom-built AI-enhanced large-signal distortion assessment tool implemented as part of the 3AI approach on a low-power wide-area network chipset. The potential of the approach is also demonstrated with the expansion of circuit families, parametric ranges, distortion metrics, and re-targeting to other platforms/technologies. Recommended future work targeting progressive closure of detailed micro to macro requirements for unrealizable simulation speeds in next-generation wireless ICs is also discussed.
Ongoing and recommended future work at both software and hardware levels towards closing the gap between the accelerating speed capability of next-generation wireless chipsets and the necessarily extensive duration of their comprehensive AI-enhanced functional validation are elaborated on. This includes the scaling-down of the performance-estimation transistor circuit model representation refinement and further speed acceleration of the best-performing surrogate model-based design space exploration techniques, together with fabricating multi-task prototyping hardware and embedding them with critical analysis, HW/SW self-optimizing and self-paced transfer learning assets.

10. Challenges and Limitations

With the advent of complex wireless systems-of-systems, there is increasing sensitivity to small movement in the black boxes that are high-frequency chipsets. The desire is for the whole system to be sensitive to change and to build-in system design assurance. This includes: 1) An ability to sense change, when it occurs, in the unnatural signatures of the system behaviour as a change affects the high-frequency components; 2) An ability to use automatic reconfiguration machinery, model building, and fault-tolerance algorithms, with a write-once system signature for go-no-go investigation of critical change and high-frequency components; 3) A desire for intervention at the appropriate level of granularity. All these requirements present a fresh challenge for signal integrity assessment AI in an era that is not settling into rule-based machine learning and for which there is no clear industrial standardisation .
Language-based tools are maturing and building proprietary knowledge bases in deploying applications. Some industrial experience is capitalising on this knowledge. Self-supervised, transfer, and metastability training develop and ensure interpretability and auditability of the AI on which things become more sensitive. AI-enhanced signal integrity assessment must be embedded within AI vigilance; one must have mechanisms for continual integrity vigilance as vigilance increases with the degree to which loss of integrity matters.
The co-existence of an AI-enhanced signal integrity assessment, AI-Vigilance, and a model of deployment knowledge might provide constraints for new AI-build machine-learning algorithms in the area of signal integrity assessment. Even with fresh ideas, some course ideas need to be borne in mind: exploratory wargaming, competition, and diverse thinking must be included to ensure an idea space that remains fresh and relevant. The key would be to identify agile AI-enhanced signal integrity assessment with innate AI vigilance and to ensure that both are at the right level of granularity, covert and diverse.

10.1. Data Quality Issues

Communication systems, such as cellular or satellite systems, mostly rely on wireless air-interface for service provisioning. From subscriber stations to gateways or base stations, data travels through various communication links, undergoing modulation and demodulation processes. As wireless receivers may experience fading or interference, received signal samples are acquired as the input of artificial intelligence (AI) algorithms for reducing computation burden at the network core. As signal characteristics differ with the communication standards, the agreement of input databases with the trained AI receiver is critical for the successful deployment of AI algorithms in practical systems. Therefore, a quality assessment framework is needed to ensure the compatibility between input demonstrations and AI-enabled transceivers. A framework for dataset quality assessment of machine learning (ML) models in wireless communications is proposed.

Data quality is not self-evident due to the unreliability of sources or errors incurred during transmission, transfer, or storing of data-related artifacts. Data to an application might be representation of the reality of significantly different quality, determining the reliability of any decisions taken based on it. In order to make sure that applications are fed with data of sufficient quality, these data ought to be assessed, so high-quality artifacts are guaranteed with high probability. This checking or monitoring of data quality is referred to as data quality assessment (DQA). The goal of DQA is to check whether the dataset is fit for a specified task, based on the metric of fitness [1] to be further narrowed with the clarification of both data and task types.

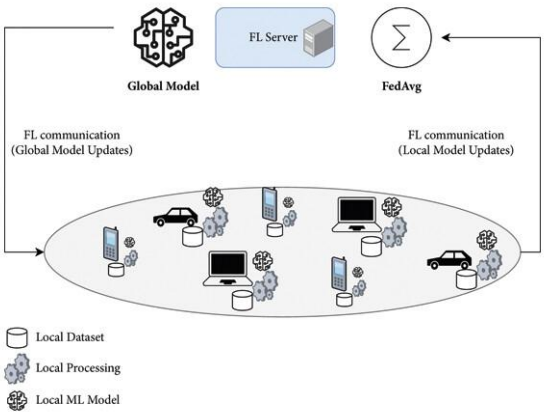

Fig 5 : Artificial Intelligence in 6G Wireless Networks

10.2. Scalability Concerns

As technology scales down to the silicon atomic limit or jumps into the 2D material arena, electromagnetic effects dominate and necessitate stringent signal integrity specifications. Advanced verification tools have been recently proposed for on-chip signal integrity robustness assessments, especially for high-frequency serial links with multiple drivers, receivers, vias, or standard-cell-based interconnects. However, the capability of existing signal integrity tools is insufficient for large-size high-frequency chipsets. This section describes three key challenges for the scalability of the presented approaches: N2-completeness of the numerical model generation, high engineering effort in device netlist preparation and CAD tool setup, and exponential complexity in the ultimate result evaluation.

RTS induction and propagation probabilities are computed in ultra-scaled layouts from the results of the tens of G-samples Monte Carlo simulations of long periods. A significant percentage of real-world test cases require a multi-day run, per snippet. The bottleneck much forbids using the comprehensive statistical parametric model-based design closure methods for the signal integrity robustness assessment. Moreover, since parametric circuit simulation is inherently an N2-complete problem, as a more realistic extension of a finite-integer-time worst-case pole extraction for clock trees to the board-design-size deterministic time-scale spectrum analysis, any parameterized numerical driven analysis in physical-domain analog layout verification is N2-complete. Hence, it is impossible to solve this problem analytically for very large real-world analog chips, demanding counteracting exhaustive semi-deterministic parallel-hybrid simulation methods.

In deep sub-micron technologies, more front-end and backend devices are assembled just-in-time in circuit blocks or chips. Each has employment guidelines and verification templates from routine tests to slice tests. Structural and parametric block tests largely ensure the hidden glitches do not propagate to drivers. Once the written layouts are integrated into a big chip design with millions and billions of component netlists, routing and graph solutions are often incomparable. Failing failures with forgotten floor plans or neglected bonds may lead to output jitter that fails the most relaxed pin-to-pin alarms. The commoditized boxed red fibs shift to prevent incorrect draining of on-chip power before thermal-cleaved clocking allowance.

11. Future Directions

In the future, AI-enhanced signal integrity assessment tools will play an increasingly crucial role in the development and evaluation of IPs for 5G and beyond applications. Therefore, the development of a metric to assess signal integrity issues of AI-enabled systems will be essential. Different from traditional schemes which assume linear signal processing systems, the new metric should take into consideration various nonlinear estimators with non-linear channel effects on received samples, random number generators, artificial noise and etc. Non-linear schematics can be represented by dynamic neural networks which can also easily capture multi-dimensional relations within high-dimensional samples. Advanced topologies for learning dynamic neural networks with stronger learning and memory capability can also be leveraged. Prior knowledge of the system can be incorporated in training AI-based systems where conventional circuits are nevertheless utilized. Non-convex optimization tools such as evolutionary strategies would provide alternative schemes to promote global optimum search for highly non-convex analog circuit design. In the future, AI hardware acceleration would be highly desired to promote energy-efficient architecture of AI-enhanced IPs. On the other hand, CAD tools for native design of AI-enabled systems, including analog and mixed-signal, are still very limited. The exploration of neural circuits to estimate any non-linear functions would require excessive efforts in large dimensions and thus knowledge in this area would be essential. In addition, developing appropriate training flows in standard EDA tools will also significantly promote the design of low-power products. Regarding the application of AI in different levels, a wide onboarding tool would also ease the large-scale application of AI in chip design.

11.1. Emerging AI Technologies

Artificial Intelligence (AI) technologies have been rapidly advancing and now encompass a set of various algorithms, tools, and applications to facilitate humans' daily lives in different tasks and industries. AI has been a very active research topic in recent years as researchers and engineers continuously explore different approaches to improve their performance and applicability in more areas. The benefits of applying AI in the field of wireless communication are of great interest to the research community, especially in recent years, as they can potentially improve workflow, peak performance, and prediction capability in signal processing, performance evaluation, network management, and many more aspects of wireless communications. AI can also be used to achieve new approaches in communication problems that have not been studied efficiently. AI has demonstrated benefits in learning complicated relationships and patterns in various applications, inspiring also the communication community to explore its use and applicability in a new paradigm shift that is more data-driven than model-based.

The design and development of wireless communication systems are complicated and require a wide variety of evaluations, tests, and optimizations to ensure signal integrity, which is commonly measured in terms of Bit Error Ratio (BER). Generally, a wireless communication system consists of a transmitter and a receiver that communicate via a channel. The transmitter first casts an Input signal using analog baseband filters and digital baseband signal processing with interpolation, digital RF up-conversion, digital-to-analog converter and analog RF circuit. Next, the casted signal propagates through a channel due to impairments, noise and scaling. Finally, the receiver reconstructs the initial signal with analog RF front-end, analog-to-digital converters, cascade of digital's in parallel on-chip, and digital baseband blocks. That's why AI could provide an upper hand on innovative and efficient algorithms to learn the full system workflow and achieve model-free test designs.

In terms of potential use case, AI is explored to assist in-chip digital filter design such as interpolation, decimation and DAC filter. Also, extensive on-cloud data prediction is proposed to improve the overall performance of a compliant waveform from simulation data. AI-enhanced signal integrity tests have been applied to perform in-chip and at-speed performance evaluations in varying schemes. The current use case focuses on improving high-level simulations of digital filters using AI to approximate the different tasks in the filters. The outcome is successfully generating scheduling heuristics that improve the simulation speed of the existing methods while keeping acceptable accuracy on the digital filters' throughput.

11.2. Potential Applications in Other Domains

The recent explosive growth of artificial intelligence (AI) technology and techniques leads to the increasing application of AI in diverse domains. With the rapid development of next-generation wireless networks, communication devices are required to have a larger number of high-frequency chips. This leads to mounting signal integrity (SI) issues for high-frequency technology. A data-driven AI technique is presented in this work for assisting the SI assessment in the SI simulation process, which is crucial in the design for next-generation high-frequency chipsets [5]. This technique may also find applications in several other areas. On-chip and on-package antennas (OPAs) are challenged in the design for 5G and beyond because of stringent SI requirements that can be complicated to analyze with conventional simulations. High-frequency chipsets are required with a larger number of on-chip and on-package antennas, and the SI issues of these high-frequency technologies are mounting. The integrated passive device (IPD) technology is one of the popular fabricating technologies for next-generation high-frequency chipsets. The modeling and simulation of these technologies are crucial for verifying the SI of high-frequency chipsets [1]. However, modeling these technologies is complex, and the simulation cost is high. A data-driven AI-enhanced SI assessment method is discussed and verified in this work. This method can improve the performance and efficiency of the existing SI simulation tools dramatically. Data-

driven AI-enhanced techniques can also find applications in the electromagnetic field, independent of the traditional circuit simulator.

12. Conclusion

In this paper, a novel AI-enhanced approach to signal integrity assessment for high-frequency chipsets is presented. Advancing next-generation wireless technology, more intelligence is being integrated into the circuits, resulting in increased complexity. Consequently, it becomes paramount to have extensive test coverage for the circuits under test (CUTs) to validate their functionality, performance, and signal integrity (SI) at a time-efficient manner with high-volume production. This work aims to expedite the signal integrity assessment for high-frequency circuit blocks through the joint works of automated scan setup generation based on the systematic classification of the signal nets across the design hierarchy and a data-driven machine learning technique to remap the test output responses. Firstly, the signal nets are examined and categorized specification-wise, allowing manageable cut-down lists of the signal nets for the most challenging high-frequency SI assessment. Secondly, a coding-decoding architecture is introduced for a parametric search over the multi-dimensional response signature space, which is practically infeasible for exhaustive search and has proven successful in the remapping of the second-order statistics of the output responses of the linear and time-invariant networks. The proposed technique can achieve a remapping with least hardware overhead compared to the original logic circuitry [11]. Moreover, a real ISILTX Penta-band LNA living up to the latest 5G standard on a 130nm SOI CMOS process is utilized in demonstration and work data, indicating a significant alleviation of the scan setup time under copious muster cuts. Meanwhile, a possible path for future enhancement of joint works with other intelligence techniques is also discussed. Embracing the continuing advances in wireless technology and next-generation communication standards, augmented intelligence is foreseen to penetrate into nearly every aspect of the design, test, and reliability for high-frequency chips, circuits, or systems in the soon future [12]. By redirecting the AI-enablement architecture and techniques, circuit-level structural/DfT designs can be mystified. Consequently, the competitiveness in terms of performance, robustness, security, etc., can be further elevated in ultrahigh performance and/or low-power tract for the faster operations and longer connections. Based on what has been covered in the previous chapters, an ending remark will be made for an extensive blueprint of the vision of the AI-enablement expansion over the high-frequency circuits test, modulation, and design co-optimization in the future design flow.

References:

1. Venkata Krishna Azith Teja Ganti, Chandrashekar Pandugula,Tulasi Naga Subhash Polineni, Goli Mallesham (2023) Exploring the Intersection of Bioethics and AI-Driven Clinical Decision-Making: Navigating the Ethical Challenges of Deep Learning Applications in Personalized Medicine and Experimental Treatments. Journal of Material Sciences & Manufacturing Research. SRC/JMSMR-230
2. Sondinti, K., & Reddy, L. (2023). Optimizing Real-Time Data Processing: Edge and Cloud Computing Integration for Low-Latency Applications in Smart Cities. Available at SSRN 5122027.
3. Malempati, M., Sriram, H. K., Kaulwar, P. K., Dodda, A., & Challa, S. R. Leveraging Artificial Intelligence for Secure and Efficient Payment Systems: Transforming Financial Transactions, Regulatory Compliance, and Wealth Optimization.
4. Chava, K. (2023). Generative Neural Models in Healthcare Sampling: Leveraging AI-ML Synergies for Precision-Driven Solutions in Logistics and Fulfillment. Available at SSRN 5135903.
5. Komaragiri, V. B. The Role of Generative AI in Proactive Community Engagement: Developing Scalable Models for Enhancing Social Responsibility through Technological Innovations
6. Chakilam, C. (2023). Leveraging AI, ML, and Generative Neural Models to Bridge Gaps in Genetic Therapy Access and Real-Time Resource Allocation. Global Journal of Medical Case Reports, 3(1), 1289. https://doi.org/10.31586/gjmcr.2023.1289
7. Lahari Pandiri, Srinivasarao Paleti, Pallav Kumar Kaulwar, Murali Malempati, & Jeevani Singireddy. (2023). Transforming Financial And Insurance Ecosystems Through Intelligent Automation, Secure Digital Infrastructure, And Advanced Risk Management Strategies. Educational Administration: Theory and Practice, 29(4), 4777–4793. https://doi.org/10.53555/kuey.v29i4.9669
8. Challa, K. Dynamic Neural Network Architectures for Real-Time Fraud Detection in Digital Payment Systems Using Machine Learning and Generative AI
9. Mahesh Recharla, Sai Teja Nuka, Chaitran Chakilam, Karthik Chava, & Sambasiva Rao Suura. (2023). Next-Generation Technologies for Early Disease Detection and Treatment: Harnessing Intelligent Systems and Genetic Innovations for Improved Patient Outcomes. Journal for ReAttach Therapy and Developmental Diversities, 6(10s(2), 1921–1937. https://doi.org/10.53555/jrtdd.v6i10s(2).3537
10. Phanish Lakkarasu, Pallav Kumar Kaulwar, Abhishek Dodda, Sneha Singireddy, & Jai Kiran Reddy Burugulla. (2023). Innovative Computational Frameworks for Secure Financial Ecosystems: Integrating Intelligent Automation, Risk Analytics, and Digital Infrastructure. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 334-371.

11. [11]Avinash Pamisetty. (2023). Integration Of Artificial Intelligence And Machine Learning In National Food Service Distribution Networks. Educational Administration: Theory and Practice, 29(4), 4979–4994. https://doi.org/10.53555/kuey.v29i4.9876
12. Pamisetty, V. (2023). Optimizing Public Service Delivery through AI and ML Driven Predictive Analytics: A Case Study on Taxation, Unclaimed Property, and Vendor Services. International Journal of Finance (IJFIN)-ABDC Journal Quality List, 36(6), 124-149.
13. Venkata Narasareddy Annapareddy, Anil Lokesh Gadi, Venkata Bhardwaj Komaragiri, Hara Krishna Reddy Koppolu, & Sathya Kannan. (2023). AI-Driven Optimization of Renewable Energy Systems: Enhancing Grid Efficiency and Smart Mobility Through 5G and 6G Network Integration. Educational Administration: Theory and Practice, 29(4), 4748–4763. https://doi.org/10.53555/kuey.v29i4.9667
14. Someshwar Mashetty. (2023). Revolutionizing Housing Finance with AI-Driven Data Science and Cloud Computing: Optimizing Mortgage Servicing, Underwriting, and Risk Assessment Using Agentic AI and Predictive Analytics. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 182-209. https://ijfin.com/index.php/ijfn/article/view/IJFIN_36_06_009
15. Lahari Pandiri, & Subrahmanyasarma Chitta. (2023). AI-Driven Parametric Insurance Models: The Future of Automated Payouts for Natural Disaster and Climate Risk Management. Journal for ReAttach Therapy and Developmental Diversities, 6(10s(2), 1856–1868. https://doi.org/10.53555/jrtdd.v6i10s(2).3514
16. Botlagunta Preethish Nandan, & Subrahmanya Sarma Chitta. (2023). Machine Learning Driven Metrology and Defect Detection in Extreme Ultraviolet (EUV) Lithography: A Paradigm Shift in Semiconductor Manufacturing. Educational Administration: Theory and Practice, 29(4), 4555–4568. https://doi.org/10.53555/kuey.v29i4.9495
17. Kaulwar, P. K., Pamisetty, A., Mashetty, S., Adusupalli, B., & Pandiri, L. Harnessing Intelligent Systems and Secure Digital Infrastructure for Optimizing Housing Finance, Risk Mitigation, and Enterprise Supply Networks
18. Srinivasarao Paleti. (2023). Data-First Finance: Architecting Scalable Data Engineering Pipelines for AI-Powered Risk Intelligence in Banking. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 403-429.
19. Kaulwar, P. K. (2023). Tax Optimization and Compliance in Global Business Operations: Analyzing the Challenges and Opportunities of International Taxation Policies and Transfer Pricing. International Journal of Finance (IJFIN)-ABDC Journal Quality List, 36(6), 150-181.
20. Abhishek Dodda. (2023). Digital Trust and Transparency in Fintech: How AI and Blockchain Have Reshaped Consumer Confidence and Institutional Compliance. Educational Administration: Theory and Practice, 29(4), 4921–4934. https://doi.org/10.53555/kuey.v29i4.9806
21. Singireddy, J., & Kalisetty, S. Optimizing Tax Preparation and Filing Services: A Comparative Study of Traditional Methods and AI Augmented Tax Compliance Frameworks.
22. Murali Malempati. (2023). A Data-Driven Framework For Real-Time Fraud Detection In Financial Transactions Using Machine Learning And Big Data Analytics. Journal for ReAttach Therapy and Developmental Diversities, 6(10s(2), 1954–1963. https://doi.org/10.53555/jrtdd.v6i10s(2).3563
23. Malempati, M., Sriram, H. K., Kaulwar, P. K., Dodda, A., & Challa, S. R. Leveraging Artificial Intelligence for Secure and Efficient Payment Systems: Transforming Financial Transactions, Regulatory Compliance, and Wealth Optimization
24. Phanish Lakkarasu. (2023). Generative AI in Financial Intelligence: Unraveling its Potential in Risk Assessment and Compliance. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 241-273.
25. Ganti, V. K. A. T., Pandugula, C., Polineni, T. N. S., & Mallesham, G. Transforming Sports Medicine with Deep Learning and Generative AI: Personalized Rehabilitation Protocols and Injury Prevention Strategies for Professional Athletes.
26. Sondinti, K., & Reddy, L. (2023). The Socioeconomic Impacts of Financial Literacy Programs on Credit Card Utilization and Debt Management among Millennials and Gen Z Consumers. Available at SSRN 5122023
27. Hara Krishna Reddy Koppolu, Venkata Bhardwaj Komaragiri, Venkata Narasareddy Annapareddy, Sai Teja Nuka, & Anil Lokesh Gadi. (2023). Enhancing Digital Connectivity, Smart Transportation, and Sustainable Energy Solutions Through Advanced Computational Models and Secure Network Architectures. Journal for ReAttach Therapy and Developmental Diversities, 6(10s(2), 1905–1920. https://doi.org/10.53555/jrtdd.v6i10s(2).3535
28. Kannan, S. The Convergence of AI, Machine Learning, and Neural Networks in Precision Agriculture: Generative AI as a Catalyst for Future Food Systems
29. Sriram, H. K. (2023). Harnessing AI Neural Networks and Generative AI for Advanced Customer Engagement: Insights into Loyalty Programs, Marketing Automation, and Real-Time Analytics. Educational Administration: Theory and Practice, 29(4), 4361-4374.
30. Chava, K. (2023). Revolutionizing Patient Outcomes with AI-Powered Generative Models: A New Paradigm in Specialty Pharmacy and Automated Distribution Systems. Available at SSRN 5136053

31. Malviya, R. K., & Kothpalli Sondinti, L. R. (2023). Optimizing Real-Time Data Processing: Edge and Cloud Computing Integration for Low-Latency Applications in Smart Cities. Letters in High Energy Physics, 2023
32. Challa, K. (2023). Transforming Travel Benefits through Generative AI: A Machine Learning Perspective on Enhancing Personalized Consumer Experiences. Educational Administration: Theory and Practice. Green Publication. https://doi. org/10.53555/kuey. v29i4, 9241.
33. Pamisetty, A. (2023). AI Powered Predictive Analytics in Digital Banking and Finance: A Deep Dive into Risk Detection, Fraud Prevention, and Customer Experience Management. Fraud Prevention, and Customer Experience Management (December 11, 2023).
34. Pamisetty, V. (2023). Intelligent Financial Governance: The Role of AI and Machine Learning in Enhancing Fiscal Impact Analysis and Budget Forecasting for Government Entities. Journal for ReAttach Therapy and Developmental Diversities, 6, 1785-1796.
35. Pallav Kumar Kaulwar, Avinash Pamisetty, Someshwar Mashetty, Balaji Adusupalli, & Lahari Pandiri. (2023). Harnessing Intelligent Systems and Secure Digital Infrastructure for Optimizing Housing Finance, Risk Mitigation, and Enterprise Supply Networks. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 372-402. https://ijfin.com/index.php/ijfn/article/view/IJFIN_36_06_015
36. Adusupalli, B. (2023). DevOps-Enabled Tax Intelligence: A Scalable Architecture for Real-Time Compliance in Insurance Advisory. In Journal for Reattach Therapy and Development Diversities. Green Publication. https://doi.org/10.53555/jrtdd.v6i10s(2).358
37. Abhishek Dodda. (2023). NextGen Payment Ecosystems: A Study on the Role of Generative AI in Automating Payment Processing and Enhancing Consumer Trust. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 430-463. https://ijfin.com/index.php/ijfn/article/view/IJFIN_36_06_017
38. Sneha Singireddy. (2023). Integrating Deep Learning and Machine Learning Algorithms in Insurance Claims Processing: A Study on Enhancing Accuracy, Speed, and Fraud Detection for Policyholders. Educational Administration: Theory and Practice, 29(4), 4764–4776. https://doi.org/10.53555/kuey.v29i4.9668
39. Sondinti, K., & Reddy, L. (2023). Towards Quantum-Enhanced Cloud Platforms: Bridging Classical and Quantum Computing for Future Workloads. Available at SSRN 5058975
40. Ganti, V. K. A. T., Edward, A., Subhash, T. N., & Polineni, N. A. (2023). AI-Enhanced Chatbots for Real-Time Symptom Analysis and Triage in Telehealth Services.
41. Vankayalapati, R. K. (2023). Unifying Edge and Cloud Computing: A Framework for Distributed AI and Real-Time Processing. Available at SSRN 5048827.
42. Annapareddy, V. N., & Seenu, A. (2023). Generative AI in Predictive Maintenance and Performance Enhancement of Solar Battery Storage Systems. Predictive Maintenance and Performance Enhancement of Solar Battery Storage Systems (December 30, 2023).
43. Kannan, S., & Saradhi, K. S. Generative AI in Technical Support Systems: Enhancing Problem Resolution Efficiency Through AIDriven Learning and Adaptation Models.
44. Sambasiva Rao Suura, Karthik Chava, Mahesh Recharla, & Chaitran Chakilam. (2023). Evaluating Drug Efficacy and Patient Outcomes in Personalized Medicine: The Role of AI-Enhanced Neuroimaging and Digital Transformation in Biopharmaceutical Services. Journal for ReAttach Therapy and Developmental Diversities, 6(10s(2), 1892–1904. https://doi.org/10.53555/jrtdd.v6i10s(2).3536
45. Murali Malempati, D. P., & Rani, S. (2023). Autonomous AI Ecosystems for Seamless Digital Transactions: Exploring Neural Network-Enhanced Predictive Payment Models. International Journal of Finance (IJFIN), 36(6), 47-69.
46. Nuka, S. T. (2023). Generative AI for Procedural Efficiency in Interventional Radiology and Vascular Access: Automating Diagnostics and Enhancing Treatment Planning. Journal for ReAttach Therapy and Developmental Diversities. Green Publication. https://doi. org/10.53555/jrtdd. v6i10s (2), 3449
47. Koppolu, H. K. R. Deep Learning and Agentic AI for Automated Payment Fraud Detection: Enhancing Merchant Services Through Predictive Intelligence
48. Anil Lokesh Gadi. (2023). Engine Heartbeats and Predictive Diagnostics: Leveraging AI, ML, and IoT-Enabled Data Pipelines for Real-Time Engine Performance Optimization. International Journal of Finance (IJFIN) - ABDC Journal Quality List, 36(6), 210-240. https://ijfin.com/index.php/ijfn/article/view/IJFIN_36_06_010
49. Recharla, M., & Chitta, S. AI-Enhanced Neuroimaging and Deep Learning-Based Early Diagnosis of Multiple Sclerosis and Alzheimer's.
50. Paleti, S. Transforming Money Transfers and Financial Inclusion: The Impact of AI-Powered Risk Mitigation and Deep Learning-Based Fraud Prevention in Cross-Border Transactions.4907-4920
51. Moore, C. (2023). AI-powered big data and ERP systems for autonomous detection of cybersecurity vulnerabilities. Nanotechnology Perceptions, 19, 46-64.
52. Jha, K. M., Bodepudi, V., Boppana, S. B., Katnapally, N., Maka, S. R., & Sakuru, M. (2023). Deep Learning-Enabled Big Data Analytics for Cybersecurity Threat Detection in ERP Ecosystems.
53. Boppana, S. B., Moore, C. S., Bodepudi, V., Jha, K. M., Maka, S. R., & Sadaram, G. (2021). AI And ML Applications In Big Data Analytics: Transforming ERP Security Models For Modern Enterprises.

54. Jha, K. M., Bodepudi, V., Boppana, S. B., Katnapally, N., Maka, S. R., & Sakuru, M. (2023). Deep Learning-Enabled Big Data Analytics for Cybersecurity Threat Detection in ERP Ecosystems.
55. Katnapally, N., Murthy, L., & Sakuru, M. (2021). Automating Cyber Threat Response Using Agentic AI and Reinforcement Learning Techniques. J. Electrical Systems, 17(4), 138-148.
56. Velaga, V. (2022). Enhancing Supply Chain Efficiency and Performance Through ERP Optimization Strategies.